Journal of Mines, Metals and Fuels, *73(4): 1147-1161; 2025. DOI: 10.18311/jmmf/2025/48130*

Print ISSN : 0022-2755

Journal of Mines, Metals and Fuels

Contents available at: *www.informaticsjournals.co.in/index.php/jmmf*

Performance Improvement of Smart Grid by Different Multi-Level Inverters and Techniques

Manoj D. Patil[1]*, Rajendra B. Madake[1], B. M. Praveen[2], Vilas S. Bugade[3], and Ganesh H. Patil[4]

[1]*Department of Electrical Engineering, ADCET, Sangli - 416301, Maharashtra, India; mdpatileps@gmail.com*
[2]*Institute of Engineering and Technology, Srinivas University, Mangaluru - 574146, Karnataka, India*
[3]*Department of Electrical Engineering, Marathwada Mitra Mandals College of Engieering, Pune - 411052, Maharashtra, India*
[4]*Department of Electrical Engineering, Dr. D. Y. Patil Institute of Technology, Pune - 411018, Maharashtra, India*

Abstract

Multi-level inverters, which outperform conventional inverters in terms of voltage control and harmonic reduction, have become essential parts of contemporary power electronics systems. Optimizing multi-level inverters' efficiency and reducing harmonic distortion by using different calculation strategies. The study aims to investigate the impact of these methods on key performance metrics, such as efficiency improvement, Total Harmonic Distortion THD reduction, voltage quality enhancement, and overall system reliability. Finding application-specific Key Performance Indicators (KPIs) and calculating the desired improvement for each KPI are the first steps in creating a Modulation Link Interface (MLI). Total Harmonic Distortion (THD), output voltage quality, efficiency, and switching frequency are typical KPIs for MLI applications. These measurements are essential for assessing how well the MLI system is working. Neutral Point Clamped (NPC) inverter, Flying Capacitor (FC) inverter, and Cascaded H-bridge inverter. The process of choosing and putting into practice different calculation approaches for controlling a modulation link interface, or MLI, is called implementation. These approaches include more complex ones like Space Vector Modulation (SVM), Selective Harmonic Elimination PWM (SHEPWM), and Model Prognostic Control (MPC), as well as Sinusoidal Pulse Width Modulation (SPWM) methods including SPWM, PDPWM, and APODPWM.

Major Findings: *The findings show the time-voltage relationship at 150 volts, crucial for voltage modulation in electronics. Using Python, these variations can be simulated and analysed to assess their impact on system behaviour. Future research could explore advanced computation techniques like machine learning and adaptive control for real-time performance optimization of multi-level inverters.*

Keywords: Computation Techniques, Flying Capacitor, Modulation Link Interface, Model Prognostic Control, Multi-Level Inverters, Total Harmonic Distortion

1.0 Introduction

In recent decades, MLIs have emerged as pivotal components in modern power electronics due to their ability to synthesize high-quality voltage waveforms and reduce harmonic distortion compared to conventional two-level inverters. The application domains of MLIs span renewable energy systems, electric vehicles, industrial drives, and grid-connected power systems, where they enhance system efficiency and performance[1-2]. Despite their advantages, MLIs present several challenges that necessity to be solved to maximize their efficiency and

**Author for correspondence*

applicability. One of the primary issues is the complexity involved in their control and modulation strategies, as the amount of voltage levels increases. The computational problem related to the real-time implementation of these strategies poses significant challenges, impacting both hardware cost and system performance[3-4]. Moreover, achieving optimal switching patterns to minimize losses and harmonic distortion remains a non-trivial task. The primary challenge in the process of MLIs lies in developing efficient modulation techniques that ensure minimal switching losses while maintaining high-quality output waveforms. Traditional Pulse Width Modulation (PWM) techniques designed for two-level inverters are not directly applicable due to the increased complexity and voltage levels involved in MLIs[5-6]. The computational resources required for real-time implementation of these techniques escalate with the number of voltage stages, limiting practical feasibility in high-power applications. Another critical issue is the selection of appropriate switching patterns that balance the trade-off between harmonic alteration and swapping damages[7-8].

The optimal strategy varies depending on load conditions, necessitating adaptive algorithms capable of adjusting in real time. Moreover, the reliability of these inverters under varying environmental and operating conditions remains a concern, particularly in applications where uptime and efficiency are paramount[9-11]. It stems from the pressing need to enhance the performance and efficiency of MLIs through advanced computation techniques. By addressing the computational complexity and efficiency challenges, researchers aim to unlock the full potential of MLIs in diverse applications. The overarching objective is to develop novel modulation and control strategies that not only optimize performance metrics such as Total Harmonic Distortion (THD) and efficiency but also simplify implementation and reduce hardware costs[12-14]. To challenge these tasks, numerous calculation techniques have been planned and investigated. These include Artificial Intelligence (AI)-based algorithms ML and neural networks for real-time modulation and control, as well as optimization algorithms like genetic algorithms and particle swarm optimization to find optimal switching patterns[15-17]. Advanced DSP methods and FPGAs are leveraged to improve computational efficiency and achieve faster execution times. These efforts have shown promising results in condensed THD, improved efficiency, and enhanced reliability of MLIs across different operational scenarios[18-20]. By integrating advanced computation techniques, researchers have been able to mitigate the inherent challenges associated with MLIs, laying the path for their broader adoption in various power electronic applications. The pursuit of enhancing the performance of multi-level inverters through innovative computation techniques is pivotal for advancing the field of power electronics[21-23]. By speaking the tasks related to modulation complexity, switching pattern optimization, and computational efficiency, researchers aim to not only improve the functionality of MLIs but also contribute to the sustainability and efficiency of modern power systems. This paper explores these themes in depth, presenting a complete summary of the present research landscape and future directions in this critical area of study[24,25]. The remaining sections are arranged as follows: The literature review was discussed in Section 2, the proposed technique was described in Section 3, the results were discussed in Section 4, and the paper's conclusion was described in Section 5.

2.0 Literature Survey

The literature survey for presentation improvement of multi-level inverters with different computation techniques focuses on exploring existing research and advancements in enhancing efficiency, reducing harmonic distortion, and optimizing control strategies. Bano *et al.*,[26] investigate control strategies for a multi-level inverter utilizing POD and APOD pulse width modulation techniques to optimize output voltage waveforms with reduced Total Harmonic Distortions (THDs) for applications in HVDC and FACTS systems. APOD PWM effectively lowers output current THD to 15.67%, while POD PWM results in higher THD at 18.06% for voltage and 15.45% for current waveforms, highlighting APOD's superior performance in harmonic distortion reduction. Sengamalai *et al*[27] aimed to enhance the performance of multi-level inverters by reducing harmonic distortion and voltage stress through novel topologies with fewer power switches, specifically focusing on a 15-level configuration for renewable energy applications. The planned 15-level inverter with condensed switch count (10 switches) achieves significant reductions in THD (4.56%) and common-mode voltage, validated through simulations

and hardware implementation, surpassing conventional cascaded H-bridge inverters with 28 switches in efficiency and harmonic mitigation. Sengolrajan *et al*[28] examine the presentation of a DDSRF system using a 9-Level Cascade Multi-Level Inverter (NLC-MLI) for Shunt Active Filter (SAF) applications. It focuses on improving compensation power generation accuracy under unbalanced conditions using a State Delay Controller (SDC). The DDSRF system with NLC-MLI recompenses for unstable masses by addressing positive, negative, and zero sequences, and harmonic components of instantaneous active and reactive power. The proposed SDC reduces signal delay, enhancing compensation accuracy as demonstrated through MATLAB/Simulink simulations and experimental validation. Qasim *et al*[29] aimed to design and simulate a seven-level multilevel inverter using MATLAB/Simulink, focusing on reducing harmonic distortion and optimizing energy conversion efficiency from three PV methods, with a seamless transition to a reduced level during PV system outages. The seven-level inverter achieves a significantly low THD of 1.13 %, demonstrating superior performance compared to the five-level mode at 4.19 %. The phase disposition modulation with six transporters and a single mention signal controls output voltage quality under varying PV system conditions. Karania *et al.,*[30] explore a new variation method, SMT-SHE, for an asymmetrical cascade H-bridge multilevel inverter combined with conventional rectifiers and a shunt active filter, aiming to achieve grid integration with minimized harmonics and optimized performance for sensitive loads like those in a textile factory.

Ebrahimabad *et al*[31] developed a fault-tolerant Multi-Level Inverter (MLI) using a new basic unit and Staircase Module (SM), capable of continuing operation despite open-circuit faults in switches, without redundant components. The research compares this novel structure with existing designs in terms of reliability, power switches, and operational robustness. The proposed fault-tolerant MLI demonstrates resilience against switch faults while maintaining operational efficiency and voltage regulation. Comparison with conventional structures shows reduced component redundancy and enhanced reliability, validated through MATLAB/Simulink simulations and laboratory prototypes, affirming its practical viability for industrial applications. Praveena *et al*[32] suggest a Spider Monkey Optimization Convolutional Neural Network (SM-CNN)-based 31-level Multilevel Inverter (MLI) integrated with an MPPT algorithm using Radial Basis Function Neural Networks (RBFNNs) for grid-tied Photo-Voltaic (PV) systems. It aims to enhance power quality by reducing harmonics and improving power factor through innovative converter and control strategies. The proposed MLI achieves an important decrease in THD to 2.45 % while enhancing power factor and reactive power balance in grid-tied PV systems. Integration of an Integrated Boost Flyback Converter (IBFC) for DC voltage generation minimizes switching losses, validated through MATLAB/Simulink simulations for effective power quality improvement. Mahafzah *et al*[33] introduce a simplified modulation technique for a 3-level FCMLI to enhance control efficiency and facilitate broader integration into power electronic systems. The proposed technique combines SPWM with high-frequency square wave pulses to achieve balanced energy distribution across coupling capacitors, simplifying control with reduced voltage references and switching complexity, validated through simulation and analysis. Niazi *et al*[34] introduce a voltage boost SCMLI based on a CFDVM, aiming to enhance voltage gain control and power quality using the SHE technique while minimizing component count and improving economic feasibility. The proposed SCMLI structure with CFDVM achieves higher voltage gain and reduced component count compared to existing SCMLIs. High-frequency operation reduces capacitor sizes, ensuring consistent output impedance across voltage levels. Experimental validation of a 13-level prototype confirms improved efficiency and cost-effectiveness, demonstrating practical viability for industrial applications. Manivel *et al*[35] developed a Switched Capacitor (SC)-based MLI with reduced components, maintaining constant capacitor voltages, achieving higher voltage gain, and minimizing Total Standing Voltage (TSV) for improved affordability and effectiveness in solar energy applications. The proposed SC-MLI structure demonstrates reduced component count, lower TSV, and comparable THD under various conditions compared to a 17-level MLI. Experimental validation confirms operational viability and adherence to IEEE standards, highlighting its potential for efficient power conversion in renewable energy systems.

3.0 Research Proposed Methodology

Enhancing the performance of multi-level inverters involves the integration of advanced computation techniques to optimize efficiency and output quality. This approach includes the application of MPC and Artificial Intelligence (AI) algorithms, such as neural networks and genetic algorithms, to improve the inverter's dynamic response and reduce harmonic distortion. By implementing real-time monitoring and AC approaches, the methodology aims to attain greater control conversion efficiency and better voltage regulation. Additionally, the use of DSP and Field-Programmable Gate Arrays (FPGAs) enables precise and fast computation, ensuring robust performance under varying load conditions. This comprehensive strategy seeks to address the limitations of traditional control methods, providing a scalable solution for modern power electronics applications.

Figure 1 displays that Multi-level inverters (MLIs) are pivotal in modern power electronics, offering enhanced performance through various topologies such as NPC, Flying Capacitor (FC), and Cascaded H-bridge (CHB) inverters. These topologies facilitate higher voltage levels, improved efficiency, and reduced harmonic distortion. To evaluate their performance, MLIs can be assessed using both simulation and hardware validation. Advanced computation techniques such as SPWM, which generates output voltage with minimal harmonic distortion, SHEPWM, and Model Predictive Control (MPC) are employed to enhance the control and output quality. Quantified target metrics, such as THD and efficiency, are essential for comprehensive performance evaluation. The implementation of these techniques ensures optimal functioning and reliability of MLIs in various applications, bridging the gap between theoretical models and practical execution through rigorous testing and validation processes.

3.1 MLI with Quantified Target Metrics

The first step in implementing a Modulation Link Interface (MLI) is to recognize KPIs specific to the application and quantify the desired improvement for each KPI. Common KPIs for MLI applications include THD, output voltage quality, efficiency, and switching frequency. These metrics are crucial in evaluating the presentation of the MLI system. For instance, THD measures the distortion of the output waveform, while output voltage quality assesses the system's ability to regulate voltage accurately and respond to transient events. Efficacy is the amount of control damage, which directly affects the system's overall energy consumption. By quantifying the desired improvement for each KPI, you can set clear targets for the MLI design and development process, ensuring that the system meets the specific requirements of your application.

3.1.1 Modulation Link Interface (MLI)

MLI topologies are a cost-effective answer for several businesses for their numerous assistances. It is composed

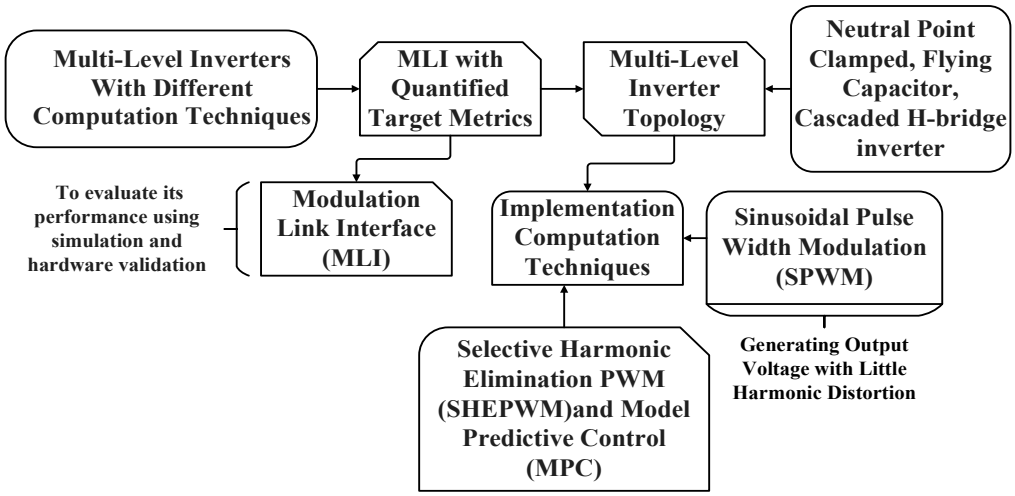


Figure 1. Block diagram of the proposed work.

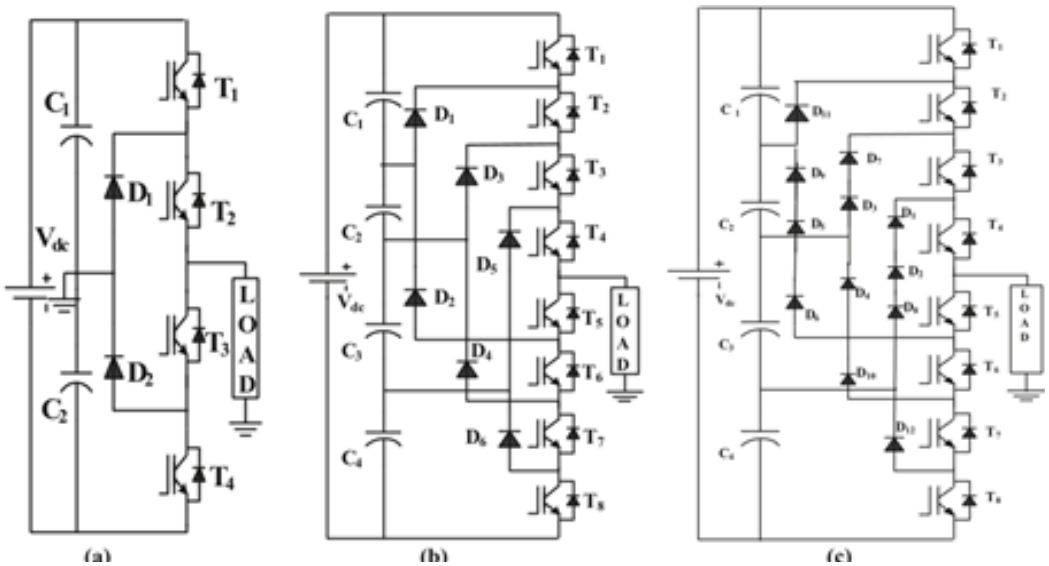


Figure 2. **(a)** Traditional 3-level diode clamped MLI. **(b)** 5-level diode clamped MLI. **(c)** 5-level improved diode clamped MLI.

of semiconductor devices and DC sources, the number of which is determined by the configuration's structure and output voltage level. The three most recognized MLI topologies are Cascaded H-Bridge MLI CHBMLI, Flying Capacitor MLI FCMLI, and Diode Clamped MLI DCMLI. These days, these MLIs kinds are referred to as classic MLIs. Using a PWM process, the DCMLI configuration created the identical configuration and tested it in an experimental arrangement. It was suggested to use an enhanced DCMLI, which is different from the original DCMLI setup. It is complete up of several clamping diodes that are connected to one other and used to share the diode voltage. Additionally, it does away with the shortcomings, including the inner device's indirect clamping and the clamping diodes' numerous blocking voltages.

Figure 2 illustrates three configurations of diode-clamped Multilevel Inverters (MLIs): (a) Traditional 3-level Diode Clamped MLI, (b) 5-level Diode Clamped MLI, and (c) 5-level Improved Diode Clamped MLI. The traditional 3-level MLI uses diodes to clamp the voltage levels, creating three distinct output levels. The 5-level Diode Clamped MLI extends this concept to produce five discrete voltage levels, enhancing the output quality and reducing harmonic distortion. The 5-level Improved Diode Clamped MLI further refines this design, incorporating advanced techniques to optimize performance, reduce switching losses, and improve efficiency, making it more suitable for high-power and high-voltage applications. The CH-BMI defines the sequence joining of a single-phase H-Bridge inverter with distinct DC sources. Each H-bridge consists of 4 switches and one DC source. This architecture has fewer components needed than DCMLI and FCMLI since it does not contain clamping diodes or clamping capacitors. Because it lacks DC link capacitors, voltage balance issues are non-existent. The switches in the three-level CHBMLI structure are activated to produce the optimistic output voltage and the negative output voltage. Each H-bridge output voltage is added to create the output voltage. The DC sources need to be isolated from one another since each H-bridge's output terminals are linked in sequence. The CHBMLI produces an output voltage level that is greater and permits the use of DC causes with varying voltage magnitudes.

Many topologies have a combination of the level group portion and the polarization group portion. The inserted basic cell is combined in series to create the level generation portion, which only produces a positive half-cycle output voltage. We refer to the single-phase H-Bridge unit. The polarization group part is added to the level group part to make the polarity reversal in the output voltage. Topology which is named a CHBMLDCI is shown in Figure 6(a). A full bridge inverter and several half-bridge cells linked in sequence make up the topology.

Two unidirectional switches and a separate DC source are wanted for each half-bridge cell. This topology's primary benefit is its ability to function at both fundamental and high switching frequencies. A low switching frequency is used for full-bridge inverter switches, while a high switching frequency is used for half-bridge cells. In contrast to the conventional MLI topologies, fewer devices are needed.

3.2 Multi-Level Inverter Topology

A Modulation Link Interface (MLI) is to choose a suitable Multi-Level Inverter (MLI) topology. This involves choosing a topology that meets the specific requirements of the application, including voltage levels, power rating, and system needs. Common MLI topologies include the NPC inverter, Flying Capacitor (FC) inverter, and Cascaded H-bridge inverter. The NPC inverter utilises topology that provides high-quality output voltage with low harmonic distortion, but it may not be suitable for high-power applications due to its limited voltage rating. The FC inverter offers improved voltage quality and higher power ratings compared to the NPC inverter, but it requires more complex control algorithms. The Cascaded H-bridge inverter provides high power ratings and flexibility in voltage levels, but it may be more expensive and complex to implement. By carefully evaluating these factors, the appropriate MLI topology can be selected to meet the specific needs of the application, ensuring optimal performance and efficiency.

Neutral Point Clamped (NPC) Inverter: The NPC inverter is renowned for its capability to generate high-quality output voltage characterized by minimal harmonic distortion, which is crucial in applications where maintaining low voltage stress on components is paramount. Its design involves multiple capacitors and switches arranged to create multiple voltage levels, ensuring smoother voltage waveforms compared to conventional inverters. However, despite these advantages, the NPC inverter is limited in voltage rating, which restricts its applicability in high-power environments requiring higher voltage levels. This limitation arises from the inherent design constraints of the clamping capacitors and switches, which may not support the voltage levels necessary for grid-tied applications or high-power industrial systems. Therefore, while ideal for applications prioritizing LHD and high voltage quality, engineers must consider its voltage limitations when selecting an appropriate inverter topology for specific high-power requirements.

Flying Capacitor (FC) Inverter: The FC inverter represents an advancement over the NPC inverter by enhancing both voltage quality and power ratings. This topology achieves improved performance through the use of flying capacitors, which enable a broader range of output voltage levels compared to the NPC configuration. The FC inverter's ability to balance capacitor voltages contributes to better voltage quality, reducing harmonic distortion and enhancing overall output waveform fidelity. Despite these benefits, the management of capacitor voltages necessitates more intricate control algorithms, which can escalate system complexity and increase design challenges. Engineers must carefully weigh these considerations against the specific application requirements to determine whether the FC inverter's advantages in voltage flexibility and quality outweigh the complexities introduced by its control and implementation needs.

Cascaded H-Bridge Inverter: The Cascaded H-Bridge inverter topology is highly regarded for its capability to deliver high power ratings and exceptional flexibility in voltage levels, catering effectively to a diverse array of applications such as high-power systems and grid-connected environments. Each H-bridge module within this topology operates independently, enabling precise control over output voltages and offering robust

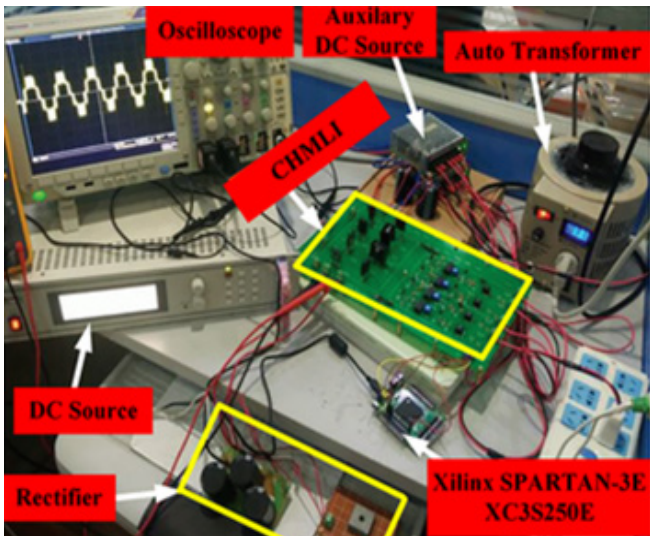


Figure 3. The Cascaded H-bridge multilevel inverter experimental system setup.

fault tolerance. This modular design not only enhances reliability but also facilitates scalability, making it adaptable to varying power demands and operational requirements. However, the cascaded structure's implementation can incur higher costs due to the improved amount needed compared to simpler inverters like NPC or FC configurations. Engineers evaluating the Cascaded H-Bridge inverter must consider these factors alongside the specific needs of their application to determine its suitability, balancing performance benefits with cost considerations for optimal system design and operation.

The selection process involves assessing parameters such as voltage levels needed, power ratings, harmonic distortion requirements, system complexity, and cost considerations. By carefully evaluating these factors against the specific needs of the application, engineers can choose the most appropriate MLI topology to ensure optimal performance, efficiency, and reliability in diverse power electronics applications.

Figure 3 illustrates an experimental setup for a Cascaded H-Bridge Multilevel Inverter (CHMLI). This system comprises several key components: a DC source that provides the direct current power, a rectifier that converts AC mains power to DC, and an autotransformer that adjusts voltage levels from the AC mains to the DC source. An oscilloscope is used to measure and visualize the CHMLI circuit. Central to the setup is the Xilinx Spartan-3E FPGA, a programmable integrated circuit that generates control signals to drive the inverter switches, synthesizing the desired AC output voltage waveform. This comprehensive configuration enables effective performance analysis and fault diagnosis of the CHMLI system.

3.3 Implementation Computation Techniques

A Modulation Link Interface (MLI) is to select and implement various computation techniques for controlling the MLI. These techniques contain SPWM methods such as SPWM, PDPWM, and APODPWM, as well as more advanced techniques like SVM, SHEPWM, and Model Predictive Control (MPC). Each process has its benefits and drawbacks, and the selection of method is subject to the precise requirements of the application. For example, SVM is effective in reducing switching losses, while SHEPWM is useful for eliminating specific harmonic frequencies. MPC offers an elevated level of flexibility and adaptability but requires a detailed model of the MLI system. Once the chosen technique is selected, it must be implemented in a simulation model, where the control algorithms and calculation methods are defined to generate the gating signals for the MLI switches. This step is crucial in verifying the presentation of the MLI below dissimilar working situations and optimizing its control strategy for optimal operation.

3.3.1 Sinusoidal Pulse Width Modulation (SPWM)

PWM is a popular modulation technique in which a sine wave reference signal is utilized to adjust the pulse train's width. Creating AC output from DC input is a typical usage for voltage source inverters.

$$PWM(t) = \begin{cases} 1, if\ sin(\omega_{carrier} t) \geq V_{ref} \\ 0, \qquad Otherwise \end{cases} \tag{1}$$

Where V_{refis} the scaled amplitude of the reference sine wave and $\omega_{carrier}$ is the carrier frequency. The harmonic removal feature of the established inflexion scheme is improved by the addition of digital filtering processes with the interpolation method. The Bessel purposes are definite in sequence increase methods in electromagnetic, telecommunication, and power methods.

$$(x) = \left(\frac{x}{2}\right)^{\propto} \sum_{k=0}^{\infty} \frac{-1^k}{k!\,\gamma(\propto +k+1)} \left(\frac{x}{2}\right)^{2k} \tag{2}$$

Where γ is the gamma function and $\propto$ is the degree of the Bessel function. The Bessel function is rearranged for $\propto = 0$ and $\propto = 1$ orders as given in the following equations:

$$j_0(x) = \sum_{k=0}^{\infty} \frac{-1^k}{2^{2k} k!\,(k+1)!} \tag{3}$$

$$j_1(x) = \left(\frac{x}{2}\right)^{\propto} \sum_{k=0}^{\infty} \frac{(-1^k) x^{2k}}{2^{2k} k!\,(k+1)!} \tag{4}$$

The corresponding integrative definition of the ordered Bessel function and the first kind. The ordinary SPWM model is another name for the basic component. The amplitude of harmonics at the carrier frequency and

multiples of carriers is distinct in the second portion of the formula. This arrangement of the Bessel function removes the carrier's sidebands and harmonics in SPWM modulation. A square wave in the time domain creates side bands on its bandwidths in the frequency domain, which are explained with function, according to modulation theory. Thus, in addition to analysing carrier harmonics, sideband harmonics of the carrier frequency must also be removed. Rendering to MT, a square wave in the time domain produces side groups on its bandwidths in the frequency domain that is described with function. Therefore, sideband harmonics of carrier frequency are required to be eliminated in addition to the carrier harmonics analysed.

3.3.2 Phase Disposition Pulse Width Modulation PDPWM

Another type of SPWM is called PDPWM, in which several carriers are employed and phase-shifted at a specific angle to one another usually 120 degrees in three-phase systems. The PDPWM modulation signals are expressed as.

$$PWM_{PDPWM}(t) = \frac{1}{2}[1 + \cos(\omega_{carrier}t + \emptyset_i)] \quad (5)$$

Where $\emptyset_i$ each carrier's phase angles are located. APODPWM is a PDPWM variant that maximizes the overlaps and pulse widths to lower harmonics and boost efficiency with modifications for asymmetrical pulse overlaps, it adheres to PDPWM's basic concepts but uses more intricate algorithms.

PDPWM has been investigated for MMC modulation; revolving transporter waves were employed to equilibrium capacitor voltages; however, it appears that they are only effective in symmetrical configurations. It is assumed for convenience that the greater and lesser arms have a total of 4 RSMs (N = 4) In addition, there are eight RSMs. Improved systems are achieved by reducing the capacitor voltage differential. It is not necessary to alter the general properties of the MMC, such as the internal circulating current, which is visible, because no further signals are supplied to the mentioned voltage. This property gives us a solid foundation on which to further reduce the circulating current.

3.3.3 Space Vector Modulation (SVM)

SVM is a more sophisticated method that synthesizes a desired output voltage vector by merging numerous voltage vectors in a two-dimensional space. It is utilized in three-phase inverters to reduce harmonics and precisely control the output voltage. The modulation signals in SVM are computed based on the location of the reference vector within the hexagonal voltage space defined by the three-phase voltages. SHEPWM with a set of nonlinear equations resulting from the Fourier series analysis of the desired waveform is solved to eliminate or decrease certain harmonics in the output waveform. MPC is a control technique that forecasts a system's behaviour over a finite period and modifies control inputs to maximize a performance index while frequently taking restrictions into account. MPC solves a cost function across a prediction horizon by using optimization techniques. Depending on the constraints and dynamics, the control input is either maximized or minimized. At the start of each switching epoch Ts, the rectifier average voltage vector vαβ, which allows cancellation of instantaneous active and reactive power tracking errors at the end of the switching period, is computed. Then, the SVM method is utilized to produce an arrangement of swapping conditions, giving a series of nearby rectifier vectors, to attain the control objective with constant switching frequency.

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} e_\alpha & e_\beta \\ e_\beta & -e_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (6)$$

Where $e_{\alpha\beta}=[e_\alpha e_\beta]^T$ and $i_{\alpha\beta}=[i_\alpha \; i_\beta]^T$ being the line voltage and current vectors in static α–β coordinates, respectively. Predictive DPC algorithms have the same power control performance in steady and transient states, except that reactive power value has a small offset in α – β reference frame. Purely sinusoidal power source voltages, eα and eβ have a sinusoidal form. Therefore, this assumption causes a small shift between line power-source voltages and input currents. If the sampling period Ts is expected to be small in comparison with the period of the power-source voltage, components of eαβ are assumed constant over the switching period (eαβ (k + 1) = eαβ (k)). As an outcome, the variation of active and reactive powers among two consecutive sampling moments can be stated as follows:

$$\begin{bmatrix} p(k+1) & -p(k) \\ q(k+1) & -q(k) \end{bmatrix} =$$

$$\begin{bmatrix} e_\alpha(k) & e_\beta(k) \\ e_\beta(k) & -e_\alpha(k) \end{bmatrix} \begin{bmatrix} i_\alpha(k+1) & -i_\alpha(k) \\ i_\beta(k+1) & -i_\beta(k) \end{bmatrix} \quad (7)$$

Predictive DPC algorithms have the same power control performance in steady and transient states, except that reactive power value has a small offset in α – β reference frame. This offset is caused by the assumption that eα and eβ are constant over the switching period (eαβ (k + 1) = eαβ (k)). However, for purely sinusoidal power source voltages, eα and eβ have a sinusoidal form.

3.3.4 Selective Harmonic Elimination PWM (SHEPWM)

SHEPWM is pivotal for enhancing multi-level inverter performance by selectively removing specific harmonic frequencies. In multi-level inverters, which utilize multiple voltage levels to approximate a sine wave, SHEPWM optimizes the switching angles of semiconductor devices to meet harmonic elimination goals. Technical implementation involves formulating and solving nonlinear equations derived from the desired output waveform's Fourier series representation. Various computation techniques such as numerical methods, optimization algorithms (e.g., genetic algorithms, particle swarm optimization), and analytical approaches are employed to control ideal switching angles. SHEPWM enhances multi-level inverter performance by reducing THD, improving power quality, and minimizing Electro-Magnetic Interference (EMI). This results in increased efficiency and reliability across applications like renewable energy systems, industrial motor drives, and grid-connected systems. Engineers utilize advanced simulation tools to validate SHEPWM algorithms, ensuring compliance with stringent harmonic standards and optimizing system performance in diverse industrial settings.

$$U'(\omega t) = \sum_{n=1}^{\infty} a_n \sin(n\omega t) \quad (8)$$

$$a_n = \frac{4}{\pi} \int_0^{\frac{\pi}{2}} U'(\omega t) \sin(n\omega t)\, d\omega t \quad (9)$$

The equation describes SHEPWM where *U(ωt)* represents the desired waveform. It utilizes a series of sinusoidal components. a_n to synthesize *U(ωt)* by controlling their amplitudes. Each a_n is determined by integrating *U(ωt)* multiplied by sin(nωt) over a fundamental period, ensuring specific harmonics are eliminated or minimized according to the SHEPWM strategy. This method allows precise control over the harmonic satisfaction of the synthesized waveform, beneficial in applications requiring low-distortion power conversion or motor control.

$$\begin{cases} \cos(\alpha_1) - \cos(\alpha_2) + \cdots \pm \cos(\alpha_C) = \dfrac{\pi}{4U} h_1 \\ . \\ . \\ \cos(n\alpha_1) - \cos(n\alpha_2) + \cdots \pm \cos(n\alpha_C) = \dfrac{n\pi}{4U} h_n \end{cases} \quad (10)$$

In SHEPWM, the equation defines the fundamental requirement to eliminate specific harmonics from multi-level inverter output waveforms. By setting the sum of cosine terms of chosen angles (α_1) equal to π/4 times an integer (U) across desired harmonics (h_1 to h_n), SHEPWM techniques can control optimum switching angles. Computational techniques like genetic algorithms or particle swarm optimization are employed to solve these nonlinear equations efficiently, achieving precise harmonic elimination while enhancing inverter performance. This approach ensures low THD and high-quality output waveforms essential for applications demanding high efficiency and minimal electrical interference.

3.3.5 Model Predictive Control (MPC)

MPC is a sophisticated control strategy used to enhance the performance of multi-level inverters by predicting future behaviour based on a dynamic model of the system. In MPC, a predictive model of the inverter's behaviour and the load dynamics is utilized to regulate optimal control actions over a finite time horizon. This predictive model takes into account system constraints, such as power and current bounds, safeguarding smooth and efficient operation. Technically, MPC iteratively computes optimal control inputs by solving a controlled optimization difficulty at each sampling time. This optimization considers both current states and future predictions, aiming to decrease a cost purpose that typically includes

objectives like tracking a reference signal and minimizing deviation from desired operation conditions. MPC enhances multi-level inverter performance by improving dynamic response, reducing harmonic distortion, and achieving precise control over production power and existing waveforms. Various computation techniques such as numerical methods, convex optimization algorithms, and real-time simulations are employed to implement MPC effectively. Engineers leverage advanced software tools for modelling, simulation, and real-time control implementation, ensuring robust performance across applications including renewable energy systems, electric vehicles, and industrial motor drives. Thus, MPC stands as a powerful approach for optimizing multi-level inverter operations while meeting stringent performance and efficiency requirements in modern power electronic applications.

$$f(\Delta u) = \sum_{j=1}^{N_P} ||y(k+j) - \omega(k+j)||^2 + \sum_{j=1}^{N_u-1} ||\Delta u\,(k+j)||^2 \quad (11)$$

In MPC, the function $f(\Delta u) = \sum_{j=1}^{N_P} ||y(k+j) - \omega(k+j)||^2 + \sum_{j=1}^{N_u-1} ||\Delta u\,(k+j)||^2$ represents the cost function optimized over a prediction horizon. Here, y (k + j) denotes predicted output at future time steps (k + j), ω(k+j) is the desired reference trajectory, and u(k + j) are the increments in control inputs over the horizon. MPC aims to minimize this cost by adjusting Δu, ensuring output y(k) closely tracks ω(k) While considering control efforts. Techniques like gradient descent or interior-point methods computationally solve this optimization, enabling precise and efficient regulation of MLI for enhanced performance in various applications.

4.0 Experimentation and Result Discussion

The performance enhancement for multi-level inverters using various computation techniques, experimentation and result discussion validating and optimizing their effectiveness. These inverters are crucial in modern power electronics for their capacity to improve voltage output value, decrease harmonic distortion, and improve efficiency related to traditional inverters. Experimental setups involve testing different modulation strategies, such as PWM or SHE, to achieve specific output requirements. Results often focus on metrics like THD, efficiency, and output waveform fidelity, demonstrating how different computational techniques influence these parameters.

Table 1. Simulation system configuration

Python Jupiter	Version 3.8.0
Operation System	Ubuntu
Memory Capacity	4GB DDR3
Processor	Intel Core i5 @ 3.5GHz

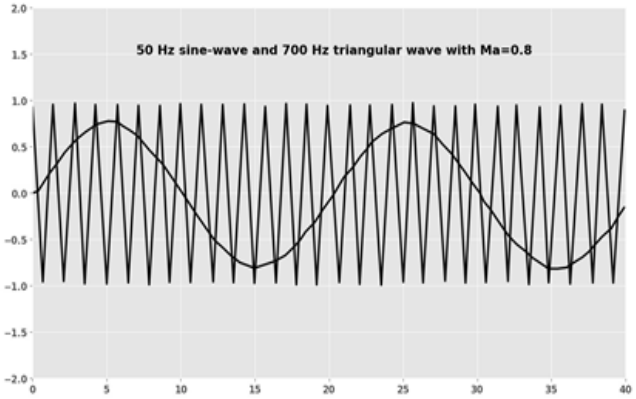


Figure 4. Composite waveform of 50 HZ sine wave and 700 HZ triangular wave with Modulation Amplitude (MA).

Python Jupiter Version 3.8.0 is installed on an Ubuntu operating system. The system has a memory capacity of 4GB DDR3 and is powered by an Intel Core i5 processor running at 3.5GHz.

Figure 4 displays a composite waveform consisting of a 50 Hz sine wave and a 700 Hz triangular wave, with a Modulation Amplitude (MA) of 0.8. The sine wave, which is the lower frequency component, is represented by smoother, more gradual oscillations, while the higher frequency triangular wave is depicted by the sharper, more rapid oscillations. The modulation amplitude indicates the extent to which the largeness of the triangular wave is modulated by the sine wave. This creates a complex waveform where the triangular wave's amplitude varies by the shape of the underlying sine wave, resulting in a

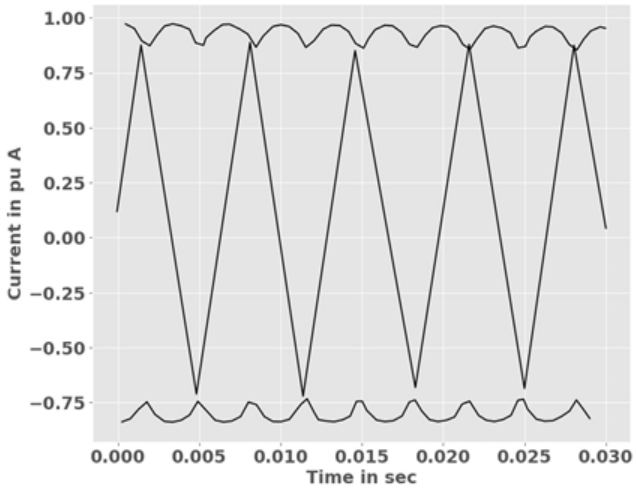


Figure 5. Modulation of high-frequency triangular wave by low-frequency signal.

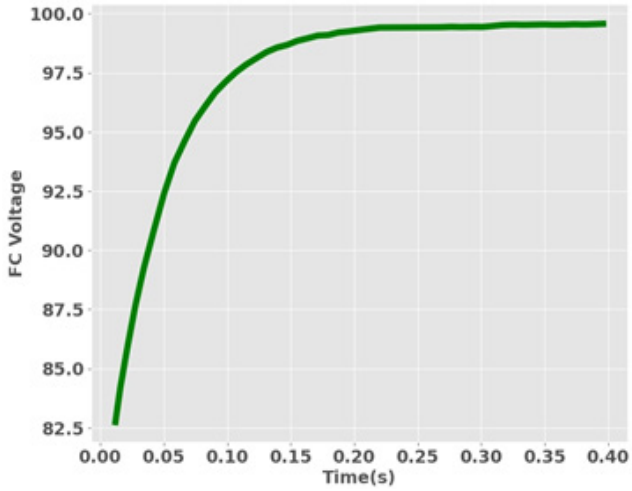


Figure 7. Frequency Modulation (FM) and its voltage-controlled carrier frequency.

visually distinctive pattern that combines both periodic signals.

Figure 5 illustrates a composite current waveform over time, highlighting a combination of high-frequency and low-frequency oscillations. The high-frequency component, represented by the rapid triangular wave, dominates the waveform with a frequency that causes several oscillations within a brief period. Superimposed on this is a lower frequency component, evident from the smoother and broader variations in the waveform's amplitude. The vertical axis indicates the current measured in per unit Amperes (pu A), while the horizontal axis represents time in seconds. The overall pattern reveals how the high-frequency triangular wave's amplitude is modulated by the lower-frequency signal, resulting in a complex waveform that varies both rapidly and gradually over time.

Figure 6 displays the modulation index and signal processing refers to a measure of the amplitude variation in a modulated signal compared to the carrier signal. For angles α_1, α_2, α_3, and α_4 with values of 1.59,

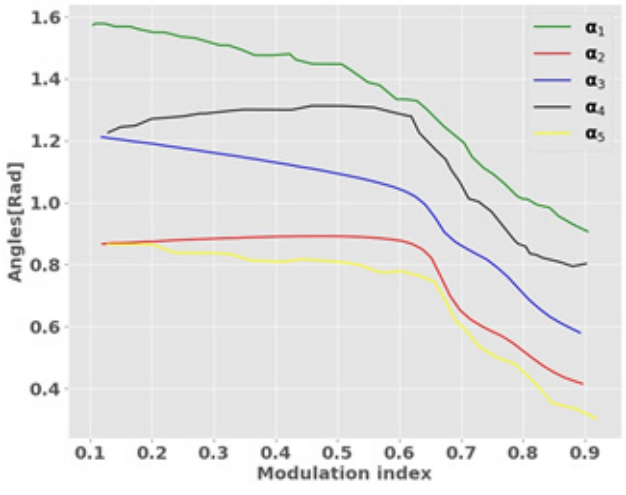


Figure 6. Understanding modulation index and its influence on signal processing.

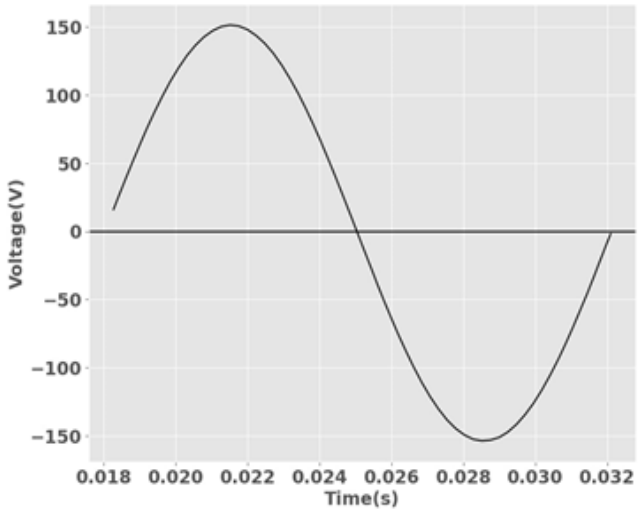


Figure 8. Temporal variations of voltage in control and modulation applications.

0.89, 1.2, and 1.230 respectively, each angle represents a phase or amplitude modulation parameter used in various modulation techniques such as PWM or Phase Shift Keying (PSK). A higher modulation index generally indicates greater deviation from the carrier signal, resulting in a more pronounced modulation effect in the transmitted or processed signal. This parameter defines signal reliability, bandwidth efficiency, and noise resilience in communication systems and power electronics applications.

Figure 7 displays the relationship between time and the Centre Frequency (Fc) voltage of 98.8 typically pertains to Frequency Modulation (FM) in communication systems or signal processing. In FM, the centre frequency is modulated by a varying voltage signal over time. A centre frequency voltage of 98.8 represents the instantaneous voltage level that determines the carrier frequency at any given moment. As this voltage changes over time, the carrier frequency shifts accordingly, resulting in a modulated signal where the frequency deviation is proportional to the amount of variation of the voltage signal. This modulation technique is utilized in radio transmission, where variations in the centre frequency enable the encoding and transmission of information as frequency variations within the carrier signal.

Figure 8 displays the relationship between time and voltage, especially with a specified value like 150, which often pertains to voltage modulation or control applications in electronics and electrical systems. In such contexts, voltage represents a crucial parameter that varies over time to regulate or modulate other electrical quantities like current or frequency. For instance, in analogue and digital circuits, a voltage of 150 volts might signify a specific control or operational condition where components or systems respond dynamically to changes in this voltage level. This relationship is fundamental in various applications ranging from power electronics to signal processing, where the temporal variation of voltage controls the behaviour or output.

Figure 9 shows in electrical engineering, when analysing the effect of load Resistance (R) on voltage THD, a load resistor's value influences how harmonics distort the purity of the voltage signal. A THD rate of 3.94 % indicates the percentage of harmonic distortion relative to the fundamental frequency in the voltage waveform. The load Resistor (R) alters the impedance characteristics, affecting how harmonics generated by non-linear loads propagate through the circuit. Higher THD values suggest more significant distortion, potentially affecting the performance of sensitive electronic equipment and requiring mitigation strategies such as filtering or using

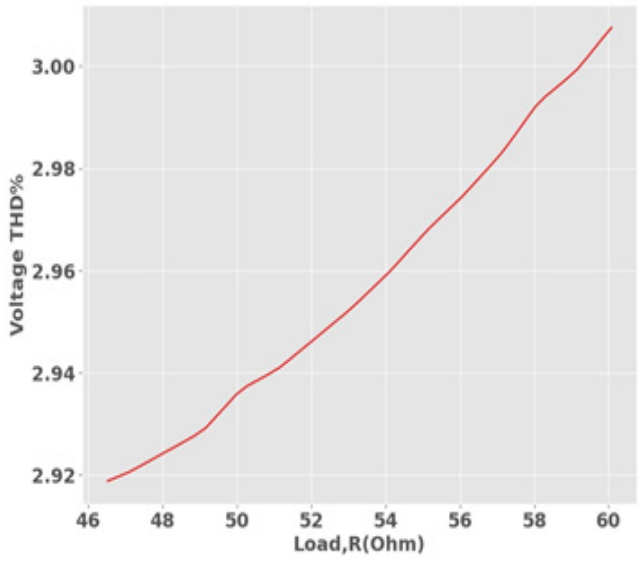


Figure 9. Impact of load resistance on voltage Total Harmonic Distortion (THD).

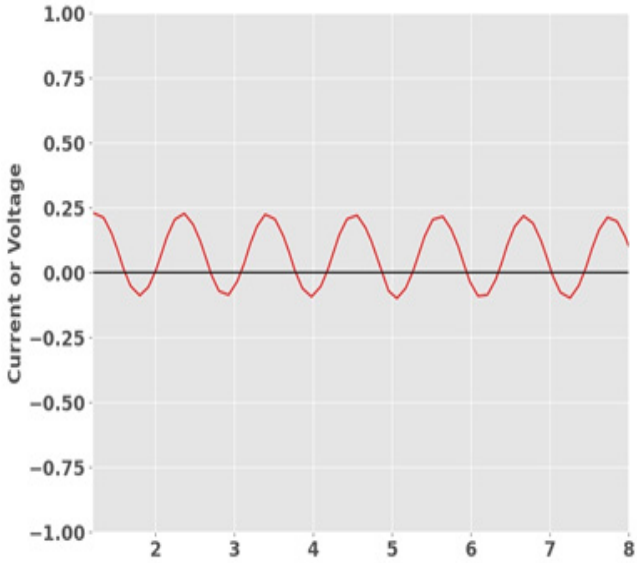


Figure 10. Interpreting current-voltage characteristics in electronic components.

higher-quality components to maintain signal integrity. Understanding this relationship is crucial in designing and maintaining reliable electrical systems, ensuring efficient power delivery, and minimizing undesirable harmonic effects.

Figure 10 shows a current-voltage (I-V) characteristic, where the y-axis represents either current or voltage, depending on the context. The red and black lines illustrate a periodic relationship concerning the x-axis values ranging from 2 to 8. Such I-V characteristics are crucial in determining the nature of electronic components: a linear relationship signifies a resistor, while non-linear behaviour indicates more complex devices like diodes or transistors. Understanding these characteristics helps in identifying and utilizing components effectively in electronic circuit design and analysis.

5.0 Research Conclusion

A broad study on refining the performance of multi-level inverters using different calculation methods has shown important discoveries and developments. Research has demonstrated that state-of-the-art modulation methods, ideal switching algorithms, and creative control schemes can successfully reduce problems like harmonic distortion and boost voltage quality, and growth system competence. The strengths and uses of these methodologies have been emphasized through comparison and analysis across various industrial and renewable energy sectors. The studies show that computational intelligence including AI and ML is increasingly being integrated to create responsive and adaptive control systems that maximize performance across a range of operating circumstances. The study emphasizes how crucial computation methods are to expanding the potential of multi-level inverters. Although there has been significant progress in optimizing performance measures through existing studies, future research initiatives should concentrate on integrating emerging technology and improving computational approaches to satisfy the changing expectations of the business. The findings show the time-voltage relationship, focusing on a significant voltage level of 150 volts, crucial for voltage modulation or control in electronics and electrical systems. Implementation of these findings using Python software involves simulating the temporal voltage variations and analysing their impact on system behaviour. Creating better-switching devices involves investigating novel semiconductor materials, creating reliable fault-tolerant control schemes, and resolving scalability concerns for extensive applications like the integration of renewable dynamism sources and electric car charging infrastructure.

6.0 References

1. Vijayakumar A, Stonier AA, Peter G, Vignesh E, Ganji V. Machine learning-based model predictive control for grid-connected Enhanced Switched Capacitor Cross-Connected Switched Multi-Level Inverter (ESC3SMLI). IET Power Electron. 2023. https://doi.org/10.1049/pel2.12546
2. Bharath Choudary V, Kavithamani A. Design of a hybrid meta-heuristic optimizer for modelling a multi-level inverter. J Nanoelectron Optoelectron. 2024; 19(6):621-33. https://doi.org/10.1166/jno.2024.3607
3. Pragathi B, Kumar S, Kumari PR, Singh AR. Performance evaluation of hybrid multilevel inverter with a high-frequency switching technique. J Eng Appl Sci. 2023; 70(1):101. https://doi.org/10.1186/s44147-023-00267-9
4. Benaouda OF, Mezaache M, Djeghloud H, Bendiabdellah A. Study of the performance of fault-tolerant multi-level inverter included in shunt active power filter. Int J Electr Comput Eng. 2023; 13(3):2471-81. https://doi.org/10.11591/ijece.v13i3.pp2471-2481
5. Shanono IH, Abdullah NRH, Daniyal H, Muhammad A. Optimizing performance of a reduced switch multi-level inverter with moth-flame algorithm and SHE-PWM. J Eng. 2023; 2023(11):12281. https://doi.org/10.1049/tje2.12281
6. Ramalingam N, Thiagarajan A. FPGA-based fault analysis for 7-level switched ladder multi-level inverter using decision tree algorithm. Int J Reconfigurable Embedded Syst. 2023; 12(2):157-64. https://doi.org/10.11591/ijres.v12.i2.pp157-164
7. Nithya R, Anitha T, Arulaalan M. Design of 243-level trinary ladder multilevel inverter using VHDL. J Surv Fish Sci. 2023; 10(2S):418-25. https://doi.org/10.53555/sfs.v10i2S.330
8. Seshadri MK, Kanipakam V. Analysis of multi-level inverters for electric vehicle application. 2023.
9. Gopinath B, Suresh S, Jayabaskaran G, Geetha M. Renewable energy resource integrated multilevel inverter using evolutionary algorithms. Automatika.

2024; 65(3):1061-78. https://doi.org/10.1080/00051144.2024.2329494
10. Parimalasundar E, Muthukaruppasamy S, Dharmaprakash R, Suresh K. Performance investigations of five-level reduced switches count H-bridge multilevel inverter. Electr Eng Electromech. 2023; (6):58-62. https://doi.org/10.20998/2074-272X.2023.6.10
11. Singh H, Srivastava D. Sentiment analysis: Quantitative evaluation of machine learning algorithms. Proc 5th Int Conf Smart Syst Invent Technol (ICSSIT). 2023.
12. Khizer M, Liaquat S, Zia MF, Kanukollu S, Al-Durra A, Muyeen SM. Selective harmonic elimination in a multilevel inverter using multi-criteria search enhanced firefly algorithm. IEEE Access. 2023; 11:3706-16. https://doi.org/10.1109/ACCESS.2023.3234918
13. Ezhilarasan G, Mohanraj K, Vishnuram P, Bajaj M, Blazek V, Prokop L, *et al*. An empirical survey of topologies, evolution, and current developments in multilevel inverters. Alexandria Eng J. 2023; 83:148-94. https://doi.org/10.1016/j.aej.2023.10.049
14. Khedekar LS. Strength of data matrix image over analysis and design of exam processing system. IEEE 8th Int Conf Converg Technol (I2CT). 2023. https://doi.org/10.1109/I2CT57861.2023.10126167
15. Ghadi YY, Iqbal MS, Adnan M, Amjad K, Ahmad I, Farooq U. An improved artificial neural network-based approach for total harmonic distortion reduction in cascaded H-bridge multilevel inverters. IEEE Access. 2023; 11:127348-63. https://doi.org/10.1109/ACCESS.2023.3332245
16. Paramasivan M, Eswaramoorthy K, Muniraj R, Kanthan PL, Babu TS, Jeevananthan S, *et al*. An alternative level enhanced switching angle modulation schemes for cascaded H-bridge multilevel inverters. IEEE Access. 2023; 11:57365-82. https://doi.org/10.1109/ACCESS.2023.3283253
17. Karthik S, Anupama AS, Deekshith SA, Santhosh L, Dhanraj M. Crypto AI: Digital nostalgic art generation using GAN and creation of NFT using Blockchain. J Emerg Technol Innov Res. 2024; 9(7):217-20.
18. Lewicki A, Kondratenko D, Odeh CI. Hybridized PWM strategy for three-and multiphase three-level NPC inverters. IEEE Trans Ind Electron. 2023. https://doi.org/10.1109/TIE.2023.3321999
19. Kala P, Jately V, Sharma A, Joshi J, Azzopardi B. ASO-based SHE method on hybrid multilevel inverter for PV application under dynamic operating conditions. IEEE Access. 2023. https://doi.org/10.1109/ACCESS.2023.3311626
20. Ramana AV, Prasad KSN, Rao AS. Predicting stages of Alzheimer's disease using fuzzy distributed ensemble learning. Afr J Biol Sci (S Afr). 2024; 6(Si2):1391-420. https://www.afjbs.com/uploads/paper/7cd10291c7603f1dd852b5cb5f474c21.pdf
21. Athimoolam A, Balasubramanian K. Fault recognition of multilevel inverter using artificial neural network approach. Intell Autom Soft Comput. 2023; 36(2). https://doi.org/10.32604/iasc.2023.033465
22. Bektaş Y. African vultures optimization algorithm-based selective harmonic elimination for multi-level inverter. Balkan J Electr Comput Eng. 2023; 11(4):329-39. https://doi.org/10.17694/bajece.1312668
23. Priya MC, *et al*. Customized semantic segmentation for enhanced disease detection of maize leaf images. Int J Recent Innov Trends Comput Commun. 2023; 11(11):31-37. https://doi.org/10.17762/ijritcc.v11i11.9074
24. Hendawi E. Multi-level inverter fed induction motors based on simplified and efficient modulation techniques. 2023.
25. Uddin MH, Abid A, Inam U, Urooj A, Siddiqui MR. A comparative analysis of a multilevel inverter topology based on phase disposition sinusoidal pulse width modulation. Eng Proc. 2023; 46(1):30. https://doi.org/10.3390/engproc2023046030
26. Bano K, Abbas G, Hatatah M, Touti E, Emara A, Mercorelli P. Phase shift APOD and POD control technique in multi-level inverters to mitigate total harmonic distortion. Mathematics. 2024; 12(5):656. https://doi.org/10.3390/math12050656
27. Sengamalai U, Ramasamy P, Thentral T, Balasubramani K, Alagarsamy M, Muthusamy S, *et al*. A simplified methodology for mitigating the harmonics and common-mode voltage using multi-level inverters for renewable energy applications. Energy Sources Part A Recover Util Environ Eff. 2023; 45(4):10449-71. https://doi.org/10.1080/15567036.2021.1980157
28. Sengolrajan T, Kalaivani C, Ashok J, Manikandan A. A novel design of 9-level cascade multi-level inverter for decoupled double synchronous reference frame in state delay controller. J Eng Res. 2023; 11(3):143-57. https://doi.org/10.1016/j.jer.2023.100106
29. Qasim MA, Velkin VI, Mohammed MF, Sammour AA, Du Y, Salih SA, *et al*. Design of a multi-level inverter for solar power systems with a variable number of levels technique. 2023. https://doi.org/10.11591/ijpeds.v14.i2.pp1218-1229
30. Karania N, Alali MA, Di Gennaro S, Barbot JP. Developed AC/DC/AC converter structure based on

shunt active filter and advanced modulation approach for asymmetrical cascade H-Bridge multi-level inverters. IEEE Open J Ind Electron Soc. 2023. https://doi.org/10.1109/OJIES.2023.3325101

31. Ebrahimabad RC, Nazarpour D, Golshannavaz S, Bolandi TG. Computer and experimental analysis of a reconfigurable staircase module-based multi-level inverter with fault-tolerant capability. ISA Trans. 2023; 143:707-22. https://doi.org/10.1016/j.isatra.2023.09.003 PMid:37696735
32. Praveena A, Sathishkumar K. Power quality improvement using a 31-level multi-level inverter with a bio-inspired optimization approach. Front Energy Res. 2024; 12:1264157. https://doi.org/10.3389/fenrg.2024.1264157
33. Mahafzah KA, Negry RM, Obeidat MA, Alsalem H. An improved modulation technique suitable for a three-level flying capacitor multilevel inverter. Int J Electr Comput Eng. 2024; 14(3):2088-8708. https://doi.org/10.11591/ijece.v14i3.pp2522-2532
34. Niazi Y, Rajaei A, Tehrani VM, Shasadeghi M, Mobayen S, Skruch P. A switched-capacitor multi-level inverter with variable voltage gain based on current-fed Dickson voltage multiplier. IEEE Access. 2023; 11:119352-61. https://doi.org/10.1109/ACCESS.2023.3327309
35. Manivel M, Kaliappan L. Analysis and implementation of switched capacitor-based multi-level inverter for electric vehicles applications. Elektron Elektrotech. 2023; 29(1):21-32. https://doi.org/10.5755/j02.eie.33053