Experimental Study of Electrochemical Etch-Stop Technique (ECE) for Achieving Better Uniformity and Precise Diaphragm Thickness

Ishita Ganjoo, Dr.Kamaljeet Singh
ishita@isac.gov.in/ishitaganjo@gmail.com
ISRO Satellite Centre, Bangalore

Abstract

In this article Electrochemical Etch Stop (ECE) technique is employed in comparison with the standard timed etch technique to etch the silicon wafer. The experiment is conducted using 6" double sided polished silicon wafer and standard CMOS steps are ollowed for the fabrication. Instead of using implantation process for electrical contacts which induces defects and stresses, etching and metal patterning is carried out to get the desired contacts. Experimental results for diaphragm thickness of 10¼m achieved by both techniques are studied. Compared to timed etch, tolerances achieved in ECE technique is better than 3¼m with good uniformity and yield. Further simulation study using T-CAD (Technology-CAD) tools is also presented in this article for optimum dose selection in creating ohmic contact for ECE technique.

Keywords: Electro-chemical etch stop (ECE), epitaxial wafer, micromachining, etching, T-CAD

1. Introduction

Bulk micromachining is the technique employed for the removal of significant amount of bulk substrate to create various MEMS structures based on diaphragm [1]. The miniaturization of these devices necessitate the requirements of dimensional control of micro-machined components such as membranes, cantilever beams, pressure sensor membranes etc. Instead of dry technique wet chemical etching is used in single crystal silicon structure to have better selectivity, faster etching rates and cost effectiveness[2]. Chemical wet etching can be further subdivided into two parts: isotropic and anisotropic wet etching to create membranes. Isotropic etching using the etchant such as HNA uniformly etches the silicon substrate in all directions i.e lateral etch rate is same as the vertical etch rate whereas anisotropic etching usesalkali solvents which are dependent on the crystallographic orientation of the silicon substrate,such as potassium hydroxide (KOH), ethylene diaminepyrocatechol (EDP), tetra-methylammonium hydroxide(TMAH) etc . This inherent property of silicon helps in realization of complex shapes as different crystallographic directions of silicon exhibited different etch rates for above etchants. Compared to other chemicals KOH is preferred choice due to non-toxicity; faster etch rates and cheaper alternative.

The major drawback in wet chemical etching technique is the control of etching process and uniform etch depth across the wafer. Standard wet etching technique employing KOH have thickness variation upto 10%. This has the detrimental effect in the realization of the pressure sensor membranes as sensitivity of the device varies as the square (for piezo-resistive sensor) or cube (for capacitive sensor) for the desired diaphragm thickness. The challenge in wet chemical etching is to have proper etch stop technique forachieving precise membrane thickness. To overcome the limitation of uncontrolled etching process and non-uniform etch depths across the wafer, generally three techniques are used: dopant etch stop, electro-chemical etch stop and dielectric etch stop [3].The major advantage of these techniques is that depth accuracy is still higher but the tolerance of the intended feature becomes independent of the etched thickness. Dopant etch stop technique is based on ion-implantation whereas a thin highly doped surface layer is formed acting as etch stop. The major limitation of this technique is the introduction of slip planes and stresses which are due to high concentration of impurities. Similarly dielectric etch stop technique employs SOI wafer

which are very expensive. Another etch stop technique is based on the p-n junction, biased by the voltage to achieve the depth control [3, 4]. Due to p-n junction formation in the initial etch stage, flow of current is blocked due to junction effect. As soon as one of the layers is etched, the oxidation takes place and etching stops. In this article both timed etch technique and ECE techniques are employed to etch the silicon wafer and experimental results are compared. 6" double sided polished silicon wafer is used for the experiments and standard CMOS steps are employed for the fabrication. Diaphragm thickness of 10¼m is targeted with the timed etch and ECE technique. Comparison of results in terms of depth and uniformity is carried out. Further, simulation study is carried out using TCAD (Technology-CAD)software MEDICI, to find out optimum dose selection for creating ohmic contacts for ECE technique.

Electro Chemical Etch Stop Technique (ECE)

ECE technique is the combination of etching technique utilizing anodic passivation characteristics of silicon by creating a reverse bias p-n junction. Epitaxial wafer (6") is used wherein positive voltage is applied directly to the n-type (front-side) and electrical contact to the p-type substrate (back-side) is established with the etch solution.Simple 4-point resistivity measurement is carried out to ensure the n- or p-type surfaces of the wafer. A voltage bias on an n-type epitaxial layer is employed to stop the dissolution of the p-type silicon substrate at the n-type epitaxial layer. This technique has the advantage of retaining all the anisotropic etching characteristics of KOH without the need for a buried p+ layer [4]. Due to sufficiently anodic biases, silicon passivizes as a result of anodic oxide formation and results in cessation of etching. Since the majority of the potential drop is across the reverse-biased p-n junction, the p-type silicon remains essentially at open circuit potential (OCP) and etches. However, with the complete removal of the p-type silicon, the diode is destroyed and the n-type silicon becomes directly exposed to the etch solution. The positive potential applied to the n-type silicon then passivizes it and etching terminates. In the present study, 3-terminal topology is used to etch the silicon. In the three terminal ECE stop technique as shown in Fig. 1, the 3 electrodes are defined as follows:

1. Metallic thin film deposited on the etched substrate (WE: Wafer Electrode) — a positive voltage is applied directly to the n-type silicon

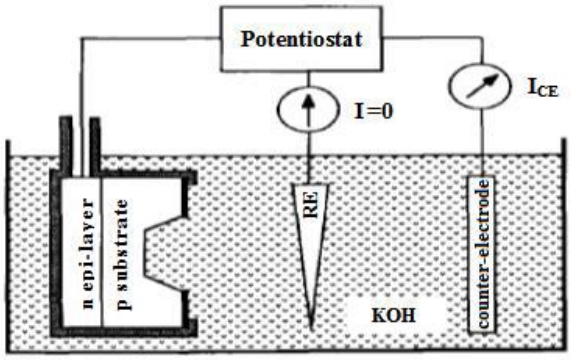


Fig. 1. Three-electrode system for etch-stop

2. Current/Counter electrode (CE) — the electrical contact to the p-type silicon is accomplished via the etch solution

3. Reference Electrode (RE) — to stabilize the potential of etchant

The bias voltage should be anodic than the oxidation formation potential (OFP) of the n type Si layer should obey,

$$V_{OFPn} < V_{bias}$$

Etching continues until the boundary of p-n junction. As the junction is reached, the reverse biased diode ceases to exist and current flows resulting in formation of anodic oxide on the n-type surface[5-6]. Thus, oxide passivizes the remaining Si after which the current reduces to a small passivation current. Observation of the peak in current just before the passivation indicates detection of the etch stop.

Experimental Details

In this work, etching is carried out by both, standard timed-etch and ECE technique in KOH bath with controlled temperature and concentration.As KOH is used for etching silicon, so patterning is carried out after the deposition of standard stack of oxide and nitride. Nitride is

deposited with the optimized recipe by tweaking pressure, power and gas flow to achieve <6% non-uniformity.

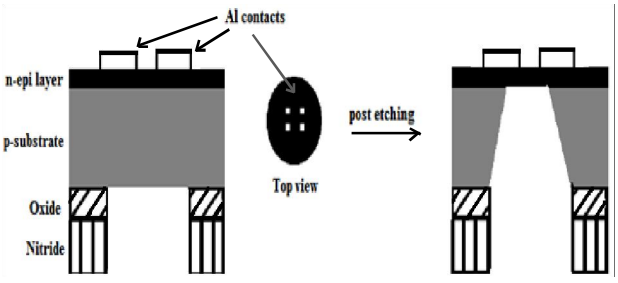
Timed etch process

Timed etching was carried out on the single side polished n type Si wafer for a target thickness of10¼m. The temperature of the KOH bath (40%conc.) was maintained at 80°C. The thickness of Si was measured periodically and subsequent constant etch rate was ensured. The remaining time required for etching was calculated accordingly for which the jig holding the wafer was immersed.

ECE process

6" epi silicon wafer is used for the experiments and standard CMOS steps are employed for the fabrication. Selective etching and sputtered aluminium is used on n-side of epitaxial wafer to get the desired contacts. Fig. 2 (a) shows the cross-section of the wafer after fabrication process.

The wafer is mounted on the jig and immersed into the etchant bath. Potential is applied to the wafer by sweeping DC voltage from -5Vto +5V and plotting the I-V characteristics. The ECE stop carried out at a reverse bias voltage of 1.5V as this value is higher than OFP of n- type Si at the given temperature. Peak current was observed indicating the complete etching away of p-substrate. The wafer was removed from the KOH bath and depth was measured using optical techniques. Fig. 2 (b) shows the cross-section of the wafer after etching process.



(a) (b)

Fig. 2 a) Cross section of epi-wafer after fabrication (cavity and Aluminium contacts) ; b) Cavity on DSP wafer after etching (Not to scale)

Observations and Results

Timed etch process

The 6'' wafer (675¼m thickness) is used and after timed-etch process, cavity depth at the major flat is measured to be 663¼mand that at the centre is measured as 661¼m; i.e. diaphragm thickness of 12¼m was achieved near the major flat and 14¼m was achieved at the centre. A standard deviation of 3.16¼m is observed.

ECE process

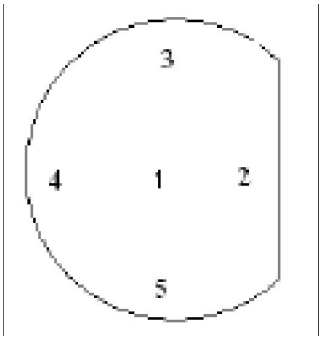


Fig. 3 Points on DSP wafer where cavity depth measurements were done

A low reverse bias value of 1.5V was selected for ECE stop such that leakage currents were less, while the bias remained anodic of passivation potential. The value of current was 20.3mA approx. at this bias. After total etching duration of 379 minutes a peak of 160mA in the current was observed. The standard deviation in thickness achieved is 1.84¼m varying from 10-13um. The measurement points are shown in Fig. 3.

Fig. 4 shows the microscopic image of the cavity with Oxide and Nitride layer walls.

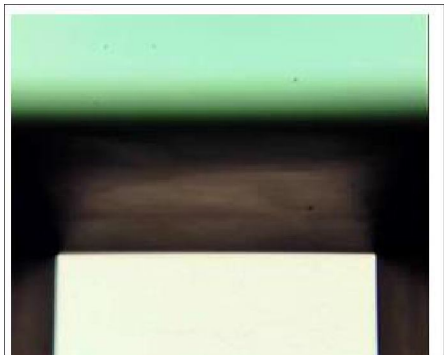


Fig. 4 Silicon diaphragm surface: microscopic image of the cavity

Discussions

The standard deviation in thickness of 1.84¼m achieved by ECE is an improvement over that of 3.16¼m achieved by timed-etch. In case of a poor p-n junction and presence of leakage currents, 4 electrode Electro chemical etch stop technique can be employed in which a fourth electrode is introduced such that the substrate is maintained at Open Circuit Potential and gets etched completely.

It was concluded that much better uniformity can be achieved by forming Ohmic contact between Aluminium and the n- type epilayer, for which the n-type Si has to be highly doped (n+ layer) to make the contact act as a resistance instead of a rectifying Schottky diode.

Simulations were carried out in MEDICI-TCAD software, to analyse the nature of the contact formed between Aluminium and the n-epi layer with changing doping concentration and its effects on the diode's characteristics.As the concentration is increased, we see that the current through the junction increases and becomes more linear in the I-V plot i.e. ohmic. In Fig.5, it is observed that on increasing doping to 5E18cm-3 characteristics approaches perfect linearity (ohmic) in the operating voltage range.

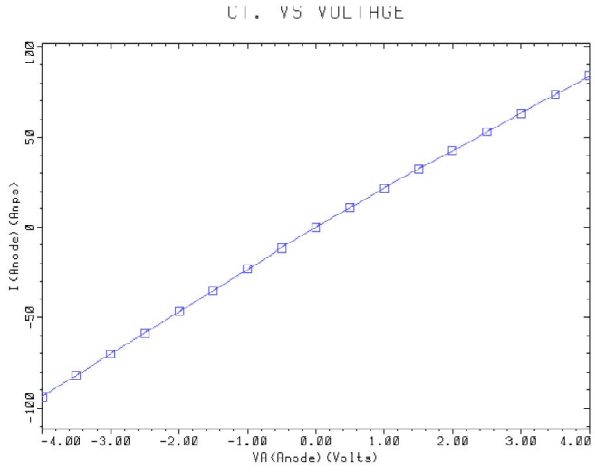


Fig. 5 I-V characteristics of Al-n type Si contact with n =5E18 cm-3 uniform doping concentration

nclusion

An experimental procedure was designed and carried out for conducting an ECE stop trial. Etch samples were fabricated and etched. The bias voltage for ECE stop, according to etching conditions of our trial, was fixed to 1.5V, determined by leaving a margin to the anodic passivation voltage found in literature. A timed etch was also carried out simultaneously on a single-side polished n type wafer for achieving the same target diaphragm thickness. It was observed that ECE-stop technique performed better with smaller variations in the target thickness. It was concluded that an ohmic Al-n contact would yield better results. Simulations on MEDICI (T-cad tool) were carried out to find the doping level required to make an ohmic Al contact.

Acknowledgement:

Authors are grateful to ISAC management for their support and encouragement. This work was carried out as part of the training assignment from IIST with the valuable support provided by SCL without which this work would not have been possible.

References

[1] K E Petersen," Silicon as a mechanical Material," Proceedings of the IEEE, Vol.70, No 5, pp 420-455, 1982.

[2] Md. Gad-el-hak, "MEMS Fabrication Literature".

[3] H. A. Waggener," Electrochemically controlled thinning of silicon," Bells System Technology J., Vol.49, No3, p473, 1970

[4] Book chapter from Handbook of Measuring System Design, J Bryzek, John Wiley & Sons, 2005.

[5] Ben Kloeck, Scott D. Collins, Nico F. Rooij and Rosemary L. Smith, "Study of