Effect of thickness on Electrical properties of anatase TiO_2 thin films by Spray Pyrolysis technique

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Abstract

The effects of film thickness on the electrical properties of anatase TiO_2 thin films deposited by spray pyrolysis were studied. The films were deposited using spray pyrolysis technique at 350°C for the time periods of 30s, 60s, and 90s and characterized for the phase and electrical characteristics. The XRD studies confirm the anatase phase of TiO_2. The electrical parameters such as ideality factor (m), zero-bias barrier height, leakage current (I_0), series resistance were obtained from the I-V characteristics of the film. The flat band voltage (V_{FB}), effective TiO_2 charge (N_{EFF}) and oxide charge concentration in TiO_2 were extracted from the high frequency C-V characteristics of the TiO_2 MOS capacitor.

Key words: TIO_2, Spray Pyrolysis, MOS capacitor, series resistance.

1. Introduction

Titanium oxide (TiO_2) has become one of the versatile, competitive and promising candidate for the applications in Ultra large scale integration (ULSI) [1], information storage, gas sensors, thin film transistor, solar cells, photo-catalysis, electronic devices and electro photographic system. The increased interest in both the application and fundamental research of this material in last decades stem from its remarkable optical and electronic properties [2, 3, 4]. A recent interest is focused on the anatase phase structure of the TiO_2 thin film which is quite applicable to humidity and gas sensors [5]. In the literature many techniques have been utilized to synthesize the TiO_2 films. Notable among them are spray pyrolysis [6,7], sputtering [3], Chemical Vapor Deposition (CVD) [8], dip coating method [9], pulsed laser deposition [10], sol–gel [11-15], atomic layer deposition [16,17]. Among all the aforementioned methods of synthesis of TiO_2 films, spray pyrolysis is quite widespread used technique due to its simplicity, commercial viability, and potential for cost-effective mass production and easy to use. Several review articles have been published in the literature highlighting the potential of this technique. In this method, desired titanium precursor is sprayed through an atomizer onto preheated substrate. Notable precursors are titanyl acetyl acetonate $(TiAcAc)[TiC_{10}H_{14}O_5]$, $Ti(i\text{-}OC_3H_7)_4$ 2-propanol,titaniumtetrachloride (TiCl4), titanium(IV) isobutoxide $[Ti((CH_3)_2CHCH_2O)]$, peroxo-titanium complex solution, etc. The properties of the thin film such as crystalline, structure, morphology, growth and electrical and optical properties are dependent upon the processing conditions and precursors used.

In the present work, we have prepared the TiO_2 thin films by spray pyrolysis technique using Titanium (IV) Isopropoxide as a precursor, Acetyl Acetonate as a complexing agent and absolute ethanol as solvent under optimized conditions [18]. The deposited TiO_2 films of different thickness were used to fabricate MOS capacitor to study the electrical properties such as

Capacitance-Voltage (C-V) and Current-Voltage (I-V). Various electrical parameters of concern were calculated from the measurements.

2. Experimental

In order to prepare the TiO_2 film, TiO_2 solution was prepared using Titanium (IV) Isopropoxide as a source material, Acetyl Acetonate as a complexing agent and absolute ethanol as solvent. The prepared solution was in the molar ratio of 0.1M. For the structural and electrical characterization, films were deposited on the p-silicon substrate. Three samples of the TiO_2 films were prepared with different spraying times of 30s, 60s and 90s at substrate temperature 350 °C under optimum conditions. For the MOS capacitor fabrication, the silicon wafer was first cleaned using RCA procedure. This step involves 15 minutes boiling of the silicon wafer at 75 °C in $NH_4OH + H_2O_2 + 6DIH_2O$ (1:1:6ml) to remove the organic contaminants, followed by 15 minutes boiling in $HCl + H_2O_2 + 6DIH_2O$ (1:1:6ml) to remove the metal contamination. The native oxide on the front surface of substrate was removed using HF: DI H_2O (BHF) in the ratio 1:10 solution and finally silicon wafer was rinsed in DI H_2O for 30s. The prepared solution was deposited onto the cleaned silicon substrates under optimum conditions. The deposited TiO_2 films were characterized through XRD technique for the phase confirmation using X-ray diffractometer (RIGAKU-MINIFLEX-II desktop) with Cu-Kα radiation (λ=1.542Å).

In order to study the electrical characteristics such as C-V and I-V of the deposited films, electrical contacts were made. Aluminum metal layer was deposited on the surface of the TiO_2 layer using thermal evaporation technique (Hindhivac vacuum coating unit Model 15F6). The dot diameter was 500µm. Before making contacts on the backside of the wafer, SiO_2 layer was etched away by using BHF solution. The front side of the wafer was covered with wax during the etching process of the backside of Si, to avoid the etching of front side TiO_2 and Al layers. After the contact was made on the back-side of the wafer, the film was dipped in Isopropyl alcohol solution to remove the wax from the front side of the wafer.

For the electrical measurements, Agilent 4155C Semiconductor parameter analyzer and Agilent 4294A precision impedance analyzer were used. The bias was applied to the back contact (Si substrate) while the top contact was kept at the ground potential. Positive and negative bias sweeps were started from zero.

3. Results and Discussion

The XRD pattern of the deposited TiO_2 film using the spray pyrolysis technique on p-silicon substrate at 350 °C is shown in Fig.1. The XRD patterns show the anatase phase of the deposited TiO_2 thin film of various thicknesses obtained by varying the deposition times of 30 s, 60 s and 90 s. The deposition conditions such as the temperature (350 °C), spray time, substrate to nozzle distance (30 cm) were optimized to achieve good quality anatase phase of TiO_2. Figure 2 shows the schematic of the fabricated Al/TiO_2/p-Silicon MOS structure.

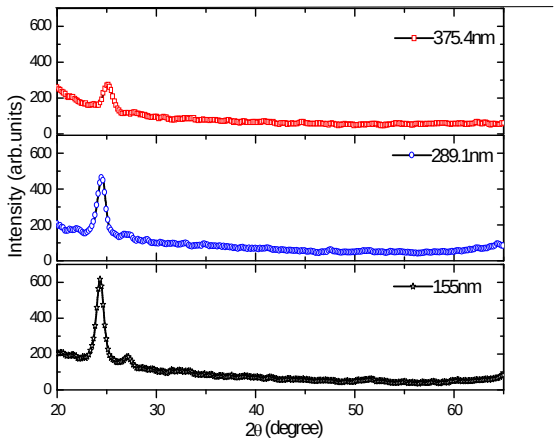


Fig 1. X-ray diffraction spectra for TiO_2 film as deposited with different thicknesses.

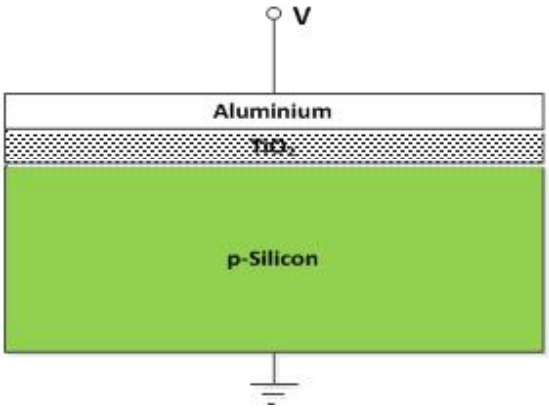


Fig 2. Al/TiO_2/p-Silicon MOS structure

Figure 3. shows the measured forward and reverse bias current and voltage characteristics of the fabricated metal-oxide-semiconductor (Al/TiO_2/ p-Si) capacitor for different TiO_2 thickness of 155nm, 289.1nm and 375.4nm. The applied voltage was varied from negative value (-4V) to positive value (+4V). Various parameters such as ideality factor (n), zero-bias barrier height, leakage current (I_0), series resistance were calculated from the Figure 3 and are tabulated in Table 1.

Ideality factor (n) for the MOS capacitor has been measured from the slope of the linear region of the forward characteristics as shown in Figure 3. The ideality factor in terms of the slope can be written as [19].

$$n = \frac{q}{kT}\left(\frac{dv}{d\ln(I)}\right) \quad \text{.....(1)}$$

Where *k* is the Boltzman constant, *T* is the temperature and *q* is the electronic charge. The high value of ideality factor is attributed to the voltage drop across the interfacial insulator layer. The values of the saturation current have been calculated by extrapolating the linear region to the ordinate. It can be seen that the large value of the leakage current in the film with TiO_2 thickness 375.4nm, is due to the large defects present in the insulating layer. The large value of defect density also affects the zero bias barrier height. The zero bias barrier height was calculated using equation,

$$\Phi_{B0} = \left(\frac{KT}{q}\right)\ln\left(\frac{AA^{*}T^{2}}{I_0}\right) \quad \text{.....(2)}$$

Where A* is the effective Richardson constant (32 A/cm^{2}K^2) for p-type silicon, A is the area of the device (1.96e-3cm^2), T is the temperature (300K), I_0 is the leakage current, q is the electronic charge, K is the Boltzmann constant. The Φ_{B0} values obtained for the MOS capacitors with different thicknesses of TiO_2 are shown in the Table 1. It was found that with the increase in TiO_2 thickness the zero bias barrier height decreases. This might be due to the increase in number of defects in the insulating layer, which lowers the barrier height with corresponding increase in the leakage current.

The series resistance (R_S) plays a crucial role in the forward I-V characteristics of the MOS structure at high applied voltage. Due to this resistance, a significant voltage drop occurs at large forward currents which reduce the voltage across the barrier. Figure 4 and 5 show the plots of Cheung functions, equations (3) and (4), extracted from forward I-V characteristics. The value of the series resistance in this work was calculated from the forward bias I–V characteristics, at high voltage, using the method developed by Cheung and Cheung [12]. Cheung functions are given as

$$\frac{dV}{d\left(\ln I\right)} = IR_S + n\left(\frac{kT}{q}\right), \quad \text{.....(3)}$$

$$H\left(I\right) = n\Phi_s + IR_S \quad \text{.....(4)}$$

The R_S value can be calculated from the slope of the curve. The calculate values of the series resistance was found to be decreasing as a function of TiO_2 film thickness. This was due to the fact that the TiO_2 film grown thermally has high interface charge density which may initiate poole frenkel emission through the insulating layer.

Table 1 Different parameters calculated from the forward and reverse characteristics of the MOS Structure

Thickness(t)	m	Φ_{B0} (I-V) (eV)	I_o(A)	R_S(dV/dln(I)) (Ω)	R_S(H(I)) (Ω)
155nm	1.78	0.7	$1.0X10^{-8}$	617.8	573
289.1nm	1.83	0.65	$7.6X10^{-8}$	143.4	142
375.4nm	3.75	0.64	$1.0X10^{-7}$	69.1	71

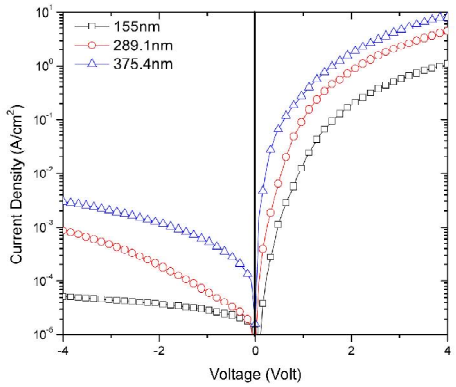


Fig 3. Forward and reverse bias current -voltage characteristic for Al/TiO_2/Si with different TiO_2 thicknesses

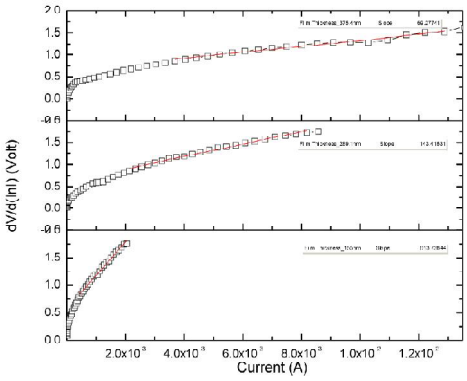


Fig. 4 $dV/d(\ln I)$-I characteristics of the Al/ TiO_2/p-silicon structure at T=300K

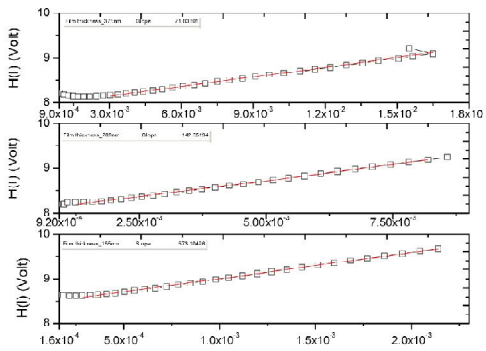


Fig. 5 $H(I)$-I characteristics of the Al/TiO_2/p-silicon structure at T=300K

In order to measure the quality of deposited oxide, C-V characteristics were measured for devices with oxide thickness of 155nm, 289.1nm and 375.4nm at 1 MHz as shown in Fig. 6. It can be seen that for all the thicknesses, MOS structure show accumulation, depletion and inversion regions of operation. The voltage corresponding to C_{min} was larger for higher value of TiO_2 film thickness. The flat band voltages (VFB), effective TiO2 charge (NEFF) and oxide charge concentration were calculated from C-V measurements. The gate dielectric thickness was extracted from the accumulation region capacitance. It can be seen that the total capacitance in the accumulation region remains constant for TiO_2 film thickness of 155nm. However, as the TiO_2 film thickness was increased, the total capacitance in the accumulation region starts decreasing if the voltage was increased beyond 2V in the negative direction. This fall in the total capacitance was due to the increase in the leakage current in the accumulation region. Therefore, it was only for TiO_2 film thickness of 155nm the strong accumulation was achieved. Therefore only for this sample, the TiO_2 oxide thickness was calculated. The calculated value was found to be 156.7nm, which was very nearly equal to the value calculated from the Ellipsometry (155nm). The flat band voltage and oxide charge concentration were obtained from the plots of $1/C^2$ versus gate voltage.

The capacitance and voltage relation for a MOS structure can be written as

$$\frac{1}{C^2} = \frac{-2V}{A^2 q \varepsilon_s N_{SUB}} \quad \ldots\ldots\ldots\ldots\ldots\ldots(5)$$

Where A is the area of the device, q is the electronic charge; N_{SUB} is the oxide charge concentration. The intercept on the x-axis, when extrapolated in the depletion region gives rise to flat band voltage. The flat band voltage calculated for the TiO_2 film thickness of 155nm, 289.1nm, 375nm were found to be -1.61V, -1.37V, -0.97V, respectively. The positive shift in the flat band voltage pertains to the increase in the defect density in the TiO_2 film thickness (375.4nm). The

oxide charge concentration can be calculated from the slope of this extrapolated line. For a film thickness of 155nm, the oxide charge concentration was found to be 1.1x 10^{16}cm^{-3}, which corresponds to resistivity (2 Ω-cm). This value was little lower than substrate resistivity (6 Ω-cm) used for the device fabrication. In the oxide layer of the practical MOS capacitor, there is always a fixed oxide charge. This charge depends upon the semiconductor orientation, oxidation and annealing conditions. It is very important for the evaluation of the wafer processes. The effective oxide charge density is the sum of the fixed oxide charge (Q_f), mobile ionic charge (Q_M) and oxide trapped charge (Q_{OT}) divided by charge.

$$N_{EFF} = \frac{Q_F + Q_M + Q_{OT}}{q} \quad \text{.....(6)}$$

For the calculation of the effective oxide charges density, the expression by Nicollian and Brews was used. It was found that the N_{EEF} was related to metal (Aluminum) - semiconductor junction and flat band voltage by [20].

$$N_{EFF} = \frac{C_{OX}\left(\phi_{MS} - V_{FB}\right)}{Aq} \quad \text{.....(7)}$$

Where A is the area, C_{ox} is the oxide capacitance per unit area, V_{FB} is the flat band voltage and ϕ_{MS} is the metal semiconductor work function difference. The calculated value for the 155nm film thickness was 1.175x10^{12}cm^{-3}.

It can be seen that other two devices with TiO_2 film thickness 289.1nm and 375.4nm show fall in the capacitance, in the accumulation region as the applied negative voltage was increased. This was due to the leakage current through the oxide. This leakage current value increases with the increase in the gate oxide thickness, as can be seen from Fig. 6. Insulating films on silicon usually contain charges which affect the semiconductor surface potential. For the fabricated devices, the hysteresis loops were observed in the C-V curves at 1MHz, as shown in Fig. 7 for two thicknesses. These characteristics match well with the previous studies of TiO_2 thin films prepared by other methods such as MOCVD [16].

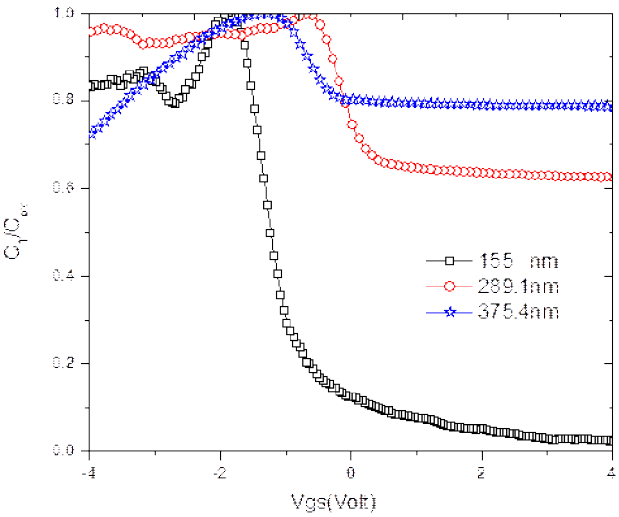


Fig.5 Normalized Capacitance -Voltage characteristic for Al/TiO_2/Si with different TiO_2 thicknesses

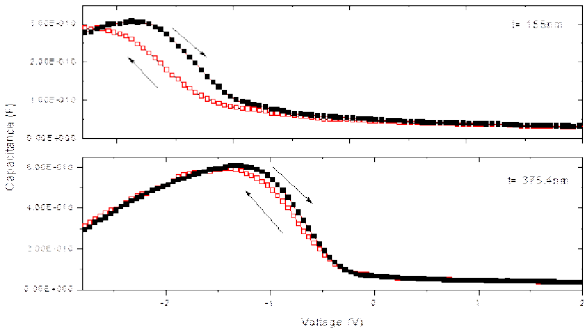


Fig.7 C-V hysteresis loop at 1 MHz of Al/TiO_2/S i with different TiO_2 thicknesses. Arrows show the direction of sweep.

Conclusion

The TiO2 thin films were deposited using spray pyrolysis technique. The effect of TiO_2 film thickness on electrical properties such as forward and reverse bias I-V and C-V characteristics of the Al/TiO_2/p-silicon MOS structures were studied. Various electrical parameters such as ideality factor, leakage current, series resistance zero bias barrier voltage and oxide charge concentration were calculated from the electrical characteristics. Experimental results reveal that

with the increase of the film thickness, the ideality factor and the leakage current increases with the corresponding decrease in the zero bias barrier height. The increase in the value of ideality factor was attributed to the potential drop in the interfacial insulator layer. The increase in the leakage current was due to the large defect densities and pinholes in the insulating layer.

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