Preparation and characterization of spray deposited CdTe thin films towards fabrication of low cost hetero-junction solar cells

R.Shashidhar, Basavaraj Angadi*, H.D.Chandra Shekar , L.C.S.Murthy

[a]Department of physics, Bangalore University, Bangalore-560056, Karnataka, India.

Abstract: Cadmium telluride (CdTe) thin films of various thicknesses (55–95 nm) were deposited through multi cycle mode on Si (100) substrates at a temperature of 350°C by spray pyrolysis technique under optimum conditions, for application as an absorber layer for hetero-junction solar cells. The structural, morphological and compositional studies of films were made through XRD, SEM and EDAX. By performing isochronal and isothermal annealing studies, resistivities of films were optimized. The estimated values of barrier height, ideality factor and reverse saturation current from M-S-M studies were found to be in the range of 0.645–0.844 eV, 0.648–10.82 and $1.309x10^{-8}$–$2.751x10^{-5}$A, respectively. The influence of CdTe film thickness on Au/CdTe/nSi/Al hetero-junction solar cell characteristics were made and the estimated cell parameters such as series resistance, shunt resistance, fill factor and efficiency were found to be in the range of 110k&!–2.66M&!, 9.3k&!–133 M&!, 25.01–26.03% and 0.00060 – 0.00020%, respectively.

Keywords: CdTe, Isochronal, Isothermal, potential barrier, solar cell, spray pyrolysis.

1. Introduction

The CdTe, a Zinc blend semiconductor [1] with a suitable direct energy band gap (1.45 eV), is a promising candidate for thin film solar cells. It is the only semiconductor of this family showing both types of conductivity [2] and having properties as those of germanium and silicon. Recently, there has been increasing interest in the fabrication of CdTe films because they exhibit useful structural, optical, electrical properties such as sensing applications [3] and remarkable solar energy conversion [4].

Solar cell is the most suitable device for the production of convenient and low cost energy. The low-cost heterojunction solar cells formed by depositing CdTe films on Si substrates have gained more attention recently. Heterojunction cells have a number of potential advantages such as an excellent blue response, simple processing steps and low processing temperatures [5]. Spray-deposited ITO films on Si substrates have relatively high conversion efficiency in 12-15% range [6]. CdTe films are preferred over ITO due to their higher conversion energy [7].

CdTe films have been prepared using several techniques such as, sputtering [8], chemical vapour deposition [9], molecular beam epitaxy [10] and spray pyrolysis [11,12]. Chemical routes of film deposition have shown great potential for photovoltaic applications because of simple and economical techniques employed [13]. Probably, the spray pyrolysis is the cheapest and elegant technique towards preparing films. Spray pyrolyzed films are of better crystalline quality, clean, adherent, denser and less porous etc., which are favourable characters for solar cell. It needs no vacuum because the films are deposited in the atmospheric ambiance. Spray-pyrolyzed CdTe films with moderate band gap, good electrical as well as optical properties and lower deposition temperature, is chosen as a potential candidate for solar cell applications [14]. Many works [15.16] pay attention to heavily doped CdTe for its potential use as solar cell absorber. The electrical transport properties of films are strongly dependent on their structure such as grain size, defects and concentration of impurities. Heat treatment affects the structure and also the resistivity of films. Hence annealing effect on film

resistivity is being taken up in the present investigation [17].

In the present investigation, intrinsic CdTe absorber layers of various thicknesses were deposited in a multi cycle mode by spray pyrolysis on n-type Si substrate to form a heterojunction solar cell. The optimization of CdTe film resistivity by annealing and influence of film thickness on solar cell electrical properties were investigated.

2. EXPERIMENTAL DETAILS

2.1 Sample preparation

Mirror-like single crystal n-type (100) Si wafer with a thickness of 350 µm and a resistivity of 1-3 &!cm, was used as a substrate in this study. Wafer cleaning is an important and critical step in device fabrication as any chemical contamination (metallic or organic) can ruin the device performance and reliability. RCA cleaning process was used for removing any particles or any chemical contaminations present on the wafer by using 2 sequential cleaning solutions, namely standard cleaning-1 (NH_3-H_2O_2-DI water in composition of 1:1:5 to remove native oxide present on the wafer) and standard cleaning-2 (HCl-H_20_2-DI water in composition of 1:1:6 to remove metal contamination on the wafer), respectively. The cleaning process was followed by a dilute HF dip and then washed with deionized water to passivate the Si dangling bonds with hydrogen. Cadmium Telluride (CdTe) thin films of various thicknesses (55-95 nm) were prepared in a multi cycle (3, 5 and 7 cycles) at various deposition time (15 s, 20 s and 25 s), by spraying 0.01 M solution of Cadmium chloride ($CdCl_2H_2O$) (Sigma Aldrich) and Tellurium oxide (TeO_2) (Sigma Aldrich) dissolved in a mixture of 1 part of ammonia solution (sp.gr.0.91 abt. 25 % extra pure S D fine chem.. ltd. India) and 4 parts of de-ionized water. 1.5 ml of Hydrazine (mono) Hydrate ($N_2H_4H_2O$) (Sigma Aldrich) is added to the solution. 1 ml of HCl is also added to the above prepared solution to get complete solubility of precursors. Thus CdTe thin films were prepared by spraying the respective precursors under optimum conditions [18] on cleaned silicon substrates maintained at a temperature of 350°C respectively.

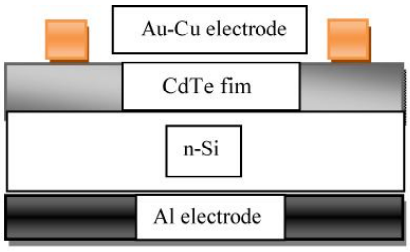


Fig.1. Cross-section of p-CdTe / n-Si hetero junction solar cells.

Au (130 nm) – Cu (18 nm) contacts were made over Si substrates which are pre-spray coated with CdTe films, by coating desired metal through a mask with an area of 1.963 x 10^{-3} cm^2 using RF sputtering technique. Anelva SPF-332H make RF sputtering unit with deposition parameters such as target to substrate distance 5.2 cm, plate voltage 1-2 kV, plate current 60-110 mA, incident power 40-150 W, reflecting power 5-25 W, pre sputtering time 5 -20 min and pressure of 6 m Torr was utilized. Aluminum films of thickness 150 nm are coated on back surface of silicon substrate using thermal evaporation technique. Hindhivac 15F6 make thermal evaporation unit with deposition parameters such as vacuum pressure 0.0752 µ Torr, boat voltage, current 20-30 V and 50 A was utilized. Film thickness was investigated using DekTak3 Profilometer and was found to vary from 55-95 nm. Fig. 1 shows the cross section of p-CdTe/n-Si solar cell. Hetero-junction solar cells were fabricated using the configuration Au/Cu/CdTe /n-Si/Al.

2.2 Sample characterization

The crystal structure of grown films was investigated using an X-ray diffraction (XRD) system with CuK_α source. The power output of the solar cell was measured using Agilent 4155C semiconductor parametric analyzer under AM1 condition. The SUSS PMS Analytical Prober was used for device probing, since probe shield protects the device from electromagnetic and radio frequency interference. Tungsten probe tips were used for probing devices.

3. RESULTS AND DISCUSSION

3.1 XRD analysis

The XRD pattern of as deposited CdTe thin films prepared by spray pyrolysis at a substrate temperature of 350°C is shown in Fig.2. Polycrystalline CdTe films show the reflections along [111], [220], [311] and [400} reflections at 2θ = 25.79°, 38.69°, 47.93° and 55.75°, respectively [19].The peaks labeled with star markers correspond to $CdTeO_3$ phase. Films grown under air ambience showed a cadmium telluride phase in addition to the cadmium telluride.

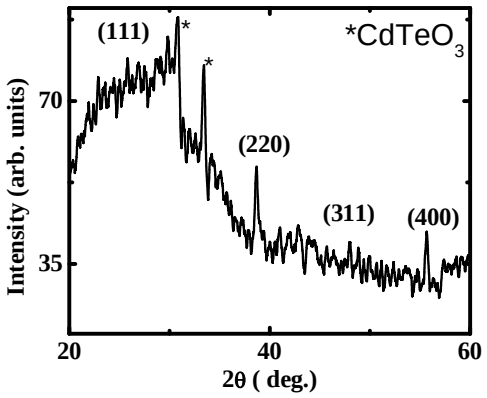


Fig.2. XRD patterns of spray pyrolized thin films.

The average grain size (D_{AG}), microstrain (ε) and dislocation density (δ) were calculated. The average grain size was estimated using the Scherrer formula,

$$D_{AG} = \frac{0.94\ \lambda}{\omega \cos \theta}, \qquad (1)$$

where λ is the wavelength of X-ray (1.54 Å) , θ is the Bragg angle and ω is the full width at half maximum (FWHM) of the XRD peaks. The microstrain (ε),

$$\varepsilon = \frac{\omega \cos \theta}{4}, \qquad (2)$$

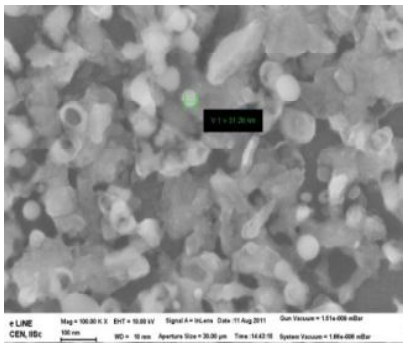
and the dislocation density (δ) defined as the length of dislocation lines per meter[3],

$$\delta = \frac{1}{D_{AG}^{2}}, \qquad (3)$$

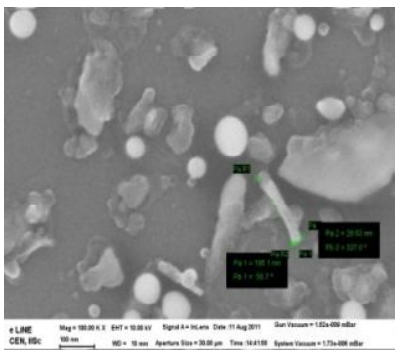
were estimated [20, 21]. The estimated average grain size (D_{AG}), microstrain (ε) and dislocation density (δ) were found to be 172 nm, 2.1 x 10^{-4} $lin^{-2}m^{-4}$ and 3.38 x 10^{13} lin m^{-2}, respectively. XRD analysis indicates that the films are crystalline and much less strained.

3.2. SEM analysis

The scanning electron micrographs (SEM) of as deposited CdTe thin films produced by spray pyrolysis at a substrate temperature of 350°C are displayed in Fig.3. The grain size of the films as estimated from SEM studies was found to be 31.26 nm. Spherical, triangular and rod like nano-structures were observed in CdTe thin film SEM patterns [CdTe (b)]. The grain size as observed from SEM is different from the average grain size that is reported from XRD. Similar kind of discrepancies was reported by Korotcenkov et al. (2005) [22] for SnO_2 films prepared by spray pyrolysis. The grains being a collection of small crystals, TEM pictures may reveal the multi nature of the grains.



(a)



(b)

Fig.3. SEM micrographs of spray pyrolized CdTe thin films.

3.3. EDAX analysis

The chemical composition of the as deposited CdTe spray pyrolized thin films was determined by Energy Dispersive X-ray Analysis Spectroscopy (EDAX). From EDAX analysis, it is found that the element weight % in CdTe are (Cd -34.39 %, Te-65.61 %), respectively. No other elemental impurities were detected in these films.

3.4. Isochronal and isothermal annealing studies

Isochronal annealing studies were made on as deposited CdTe thin films prepared by spray pyrolysis technique on Si (100) substrates. The studies were made by annealing films in air at different temperatures ranging from 100– 400°C for a constant time of 30 min. The electrical resistivity of these samples was then measured by four point probe technique (Model 280). Plot of sheet resistivity ρ_s of thin films at ambient temperature (27°C) as a function of annealing temperature is shown in fig. 4 (a). From the plot it is clear that the sheet resistivity of films found to vary between 1.455 x10^{-2} &!cm - 1.423 x10^{-2} &!cm with increase in annealing temperature from 27°C to 400° C. From the study it is also found that the sheet resistivities of films reach lowest resistivity of 1.423 x10^{-2} &!cm at annealing temperature of 400^{0}C. From the plot it is observed that in films, there is rise and fall of sheet resistivity with increase in temperature. This type of behaviour is normally observed for disordered materials. The rise in resistivity due to heat treatment in air may be associated with decrease in carrier density by filling up of oxygen vacancies and fall in resistivity may be attributed to the rearrangement and removal of defects as well as improvement in the grain structure or crystallinity.

Isothermal studies were also made on as deposited CdTe thin films by annealing at constant temperature of 400°C in air for duration ranging from 15 - 120 min. Plot of sheet resistivity ρ_s of thin films at constant temperature and as a function of annealing time is shown in fig.4 (b). From the plot it is observed that the sheet resistivity reach lower value of 1.29 x10^{-2} &!cm at 120 min (400°C) for CdTe films. The obtained films were of comparable quality of those deposited elsewhere for use as absorbing layers in solar cells.

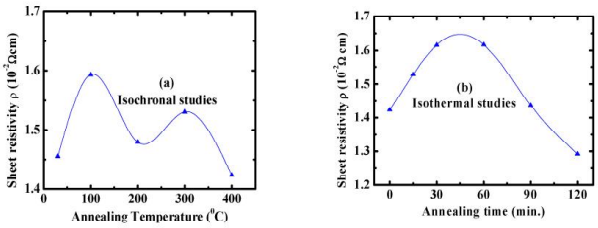


Fig.4. (a) Plot of sheet resistivity 'ρ_s' of thin films as a function of annealing temperature.

(b) Plot of sheet resistivity 'ρ_s' of thin films as a function of annealing time.

3.5. Metal-Semiconductor-Metal studies

(Au-Cu) – CdTe – (Au-Cu), MSM studies were made by probing on metal-metal contacts (inset Fig.5) of Au/Cu/CdTe/n-Si/Al configuration hetero-junction solar cells. The electrical characterization of these films was made using 4155 C semiconductor parametric analyzer. The I-V curve of the devices is drawn in fig.5. From the I-V curve, it is observed that the current increase exponentially with increase in forward bias voltage. Under forward bias (I) current flowing across a rectifying metal-semiconductor contact in a p-n junction under bias V is usually modelled as

$$I = I_s e^{\left(\frac{qV}{nk_BT}\right)}, \qquad (4)$$

Where $\left(\frac{q}{k_BT}\right)$ represents inverse thermal voltage, k_B is Boltzmann constant, n is ideality factor, T is absolute Temperature, I_s is reverse saturation current and q is electronic charge.

The Saturation current I_s is usually described within the Thermoionic emission theory of semiconductor as

$$I_s = A^* A\, T^2 e^{\left(\frac{-\varphi_b}{k_BT}\right)}, \qquad (5)$$

Where A* is the Richardson constant, A is the surface area of the diode and φ_b is the barrier height or potential. From the plot, the electrical parameters such as reverse saturation (dark) current, ideality factor and barrier potential were

evaluated using the equations (4) and (5). Estimated electrical parameters are shown in Table-1.

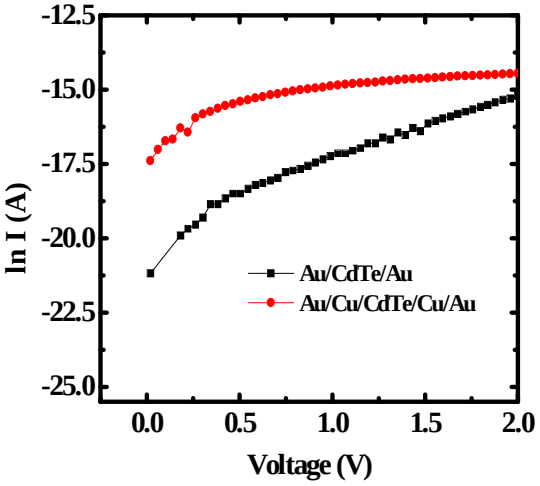


Fig.5. Plot of forward bias I-V curves.

Table 1 Estimated electrical parameters obtained from I-V studies of M-S-M structures.

M-S-M contact	Reverse saturation current I_s Acm^{-2}	Ideality factor n	Barrier potential $Ø_b$ eV
Au /CdTe/Au	2.56×10^{-7}	0.48	0.650
Au/Cu/ CdTe/ Cu/Au	2.7110^{-9}	1.60	0.768

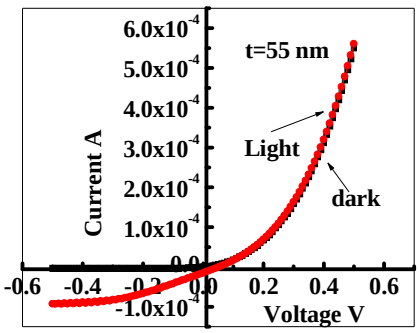
H.B.Bhuvaneswari et.al. [23] have used theoretical formulae for estimation of electrical parameters for zirconium nitride films. Lower dark current 'I_s' through the junction may be due to the trapping of charge carriers inside the pin-holes which are in plenty in spray deposited CdTe films. (Au-Cu) – CdTe – (Au-Cu), MSM structure found to possess lower reverse saturation current compared to Au – CdTe – Au which may be due to the higher value of barrier potential at the interface. Au top metal layer is preferred over ITO, since the lower reverse saturation current has lead to increase in the open circuit voltage [24] considerably at the hetero-junction.

3.6. Solar cell performance

The cells having effective area of 0.176 cm^2 were illuminated with 150 W halogen lamp. The I-V characteristics were measured and plotted in fig. 6. The dark-light I-V characteristics of cells namely Au (130nm)/Cu (18 nm150p C)/CdTe(55-95nm)/n-Si/Al(150nm,150p C) have shown excellent rectifying behaviour of hetero junction solar cells. Fig.7 shows the I-V characteristics of the hetero-junction solar cells under illumination of 206 mW/cm^2. For estimating interface states at the CdTe/Si interface, The capacitance as a function of frequency measurements were made. The values of capacitance namely, C_{LF} and C_{HF} were measured by 4155 C semiconductor parametric analyzer. From these values of capacitance, interface states (N_{is}) was estimated. The total *number* of interface states due to depletion and interface can be calculated from the capacitance measured at low frequency while the capacitance at high frequency is associated with depletion only. A lower limit of interface states N_{is} can be calculated from the relation

$$N_{is} = \left(\frac{C_{LF} - C_{HF}}{e}\right), \qquad (6)$$

Where C_{LF} and C_{HF} are the capacitance at low (50 Hz) and high (1KHz) frequencies, respectively [25].The estimated values of C_{LF}, C_{HF} and N_{is} were found to be 7.74 nF, 5.84 nF and 6.74 $\times10^{10}$Fcm^{-2}eV^{-1}, respectively. Larger number of interface states at the junction confirms the existence of large number of pin-holes at the CdTe-Si interface.



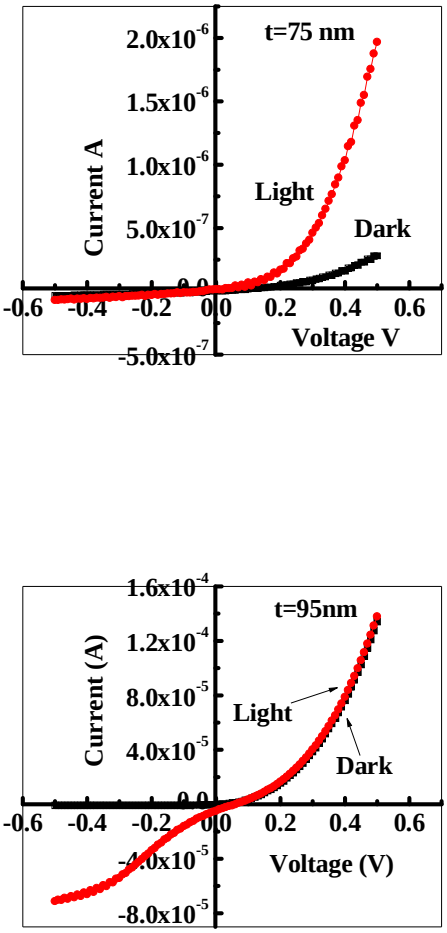


Fig. 6. Dark- light I-V characteristics showing rectifying behaviour of hetero-junction solar cells namely Au/Cu/CdTe/n-Si/Al

The estimated cell parameters under dark and light conditions using fig. 6 are shown in Table-2. The diode (ideality) factor 'n' of the cell was found to vary from 0.64-10.82, confirming that interface recombination is the dominant mechanism in these junctions. With illumination of light on the junction, dark current as well as ideality factor found to increase due to the decrement in barrier potential at the interface. As a function of thickness, dark current found to decrease with enhancement of barrier potential. However, 55 nm thick CdTe -Si performance is quite inconsistent.

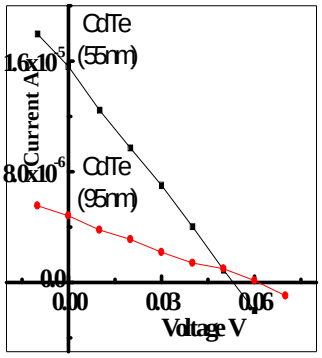


Fig. 7. I-V characteristic of the heterojunction solar cells with active area of (0.175 cm^2) under 206 mW/cm^2 illumination.

The estimated cell parameters using fig. 7 are shown in Table-3. From the study it is observed that the hetero-junction solar cells found to possess higher series resistance, lower shunt resistance, low short circuit currents (i_{sc}), low open circuit voltages (V_{OC}), small Fill Factors (FF) and consequently low efficiencies (eff). Shunt resistance may be due to recombination along the grains and large numbers of defects in spray deposited films. Lower shunt resistance not only reduces light generated current but also the

Table 2 Cell parameters under dark and light conditions

Hetero-junction Solar Cell	$I_{0(Dark)}$ µA	$Ø_{b\ (Dark)}$ eV	n_{Dark}	$I_{0(Light)}$ µA	$Ø_{b\ (Light)}$ eV	n_{Light}
CdTe(55nm) /n-Si	19.12	0.655	0.998	27.51	0.646	10.82
CdTe(75nm) /n-Si	0.013	0.844	1.478	0.050	0.809	0.648
CdTe(95nm) /n-Si	4.76	0.691	1.173	7.535	0.679	2.910

Table 3. Performance results of solar cells prepared by spray-deposition.

Hetero-junction solar cell	R_{Series} (Dark) k&!	R_{Series} (Light) k&!	Shunt (Dark) M&!	R_{Shunt} (Light) M&!	V_m mV	i_m µA	V_{oc} mV	i_{sc} µA	FF%	Eff10^{-4} %
CdTe (55nm)/n-Si	**0.354**	**0.350**	**1.1**	**0.02**	**27**	**7.99**	**53**	**15.6**	**26.03**	**5.99**
CdTe (75nm)/n-Si	**2660**	**110**	**84**	**133**	**-**	**-**	**-**	**-**	**-**	**-**
CdTe (95nm)/n-Si	**1.07**	**1.52**	**3.75**	**0.01**	**29**	**2.50**	**60**	**4.83**	**25.01**	**2.01**

open circuit voltage. Lower value of open circuit voltage may be due to pinning of donor level of n-Si at the CdTe/n-Si interface. Fill factor is found to decrease with increase in series resistance of the TiO_2 films deposited in multi-cycle at the junction. Higher series resistance may be due to the total sum of resistances at the n-Si/p- CdTe junction, (Au-Cu)- CdTe contact and (Au-Cu) as well as Al metal contacts. Lower efficiency may be due to the decrease in short circuit current, as a result of increase in barrier potential at the interface as a function of CdTe film thickness. Lower short circuit current may be due to the higher series resistance as well as trapping of charges at the multi cycle deposited CdTe films. The heat treatment process of the CdTe film coated Si substrate seriously influences the photovoltaic properties, due to the change of the surface state of Si substrate by oxidation and contamination. This may be one of the reasons for the inconsistency [26] in the photovoltaic properties of hetero-junction solar cells.

4. CONCLUSION

Cadmium telluride (CdTe) thin films of various thicknesses were successfully deposited in a multi cycle mode on Si (100) substrates at a temperature of 350°C by spray pyrolysis technique under optimum conditions for the application as the absorber layer for hetero-junction solar cells. The structural, morphological and compositional studies of these films were made by analyzing XRD, SEM and EDAX. XRD patterns shows that the films grown under air ambience showed a cadmium telluride oxide phase in addition to the cadmium telluride.SEM micrographs show spherical, triangular and rod like nano-structures in as deposited CdTe thin film. The resistivity of spray deposited CdTe films were optimized by performing isochronal and isothermal studies. The capacitance-frequency study confirms the existence of huge number of interface states due to plenty of pin-holes at the CdTe-Si interface. The influence of spray deposited CdTe film thickness on the performance of hetero-junction solar cells was made. The junctions exhibit excellent rectifying characteristics. With increase in the thickness of CdTe thin films from 55-95 nm, the power conversion efficiency (ž) found to decrease from 0.00059-0.00020%. The estimated cell parameters such as high series resistance, low shunt resistance, low fill factor and efficiencies could be attributed to higher interface states and resistivities in sprayed films. Better cell parameters could be further obtained by minimizing the spray cycles, improving the quality of sprayed films, varying the absorber thickness, reducing the resistivity of films either by further annealing in air or vacuum, doping and also by adjusting spray parameters.

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