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A novel filter for three-phase power factor correction voltage feedback loop under heavy DC voltage ripple condition

THD and the amplitude balance of three-phase input current are an important index for the performance of three-phase power factor correction (PFC). In general, when the hardware and the load of three-phase PFC are confirmed, the THD and amplitude balance of three-phase input current mainly depend on voltage and current feedback loop of PFC. Firstly, this paper designs the traditional voltage and current feedback loop for three-phase PFC according to traditional small signal theory. Secondly, this paper studies the designing difficulty of large dc voltage ripple for PFC voltage controller and puts forward a new dc voltage ripple filter which can eliminate the ac component of sampling dc bus voltage. Finally, this paper proposes a novel filter with dc voltage ripple frequency adaption function to copy with the frequency variety of the voltage ripple caused by the change of the output inverter frequency. With the help of the proposed algorithm the distortion of three-phase 3 input current reference decreases rapidly, therefore, the low THD and good amplitude balance of three phase input current will be achieved.

Keywords: *PFC, filter, harmonic, THD (total harmonic distortion)*

1. Introduction

The objective of power factor correction (PFC) is to force the input current in phase with the line voltage. Boost circuit is an excellent choice for the power stage of a power factor corrector because the inductor current of boost can be designed in continuous mode which produces the lowest level of conducted noise and the best input current waveform [1]. By the way of controlling the duty of boost circuit, the PFC feedback loop controls dc bus voltage around the dc voltage reference and forces input current in phase with the utility voltage. Therefore, the PFC feedback loop between dc voltage control and input current control has no decoupling function and has inter-disturbance between the voltage feedback loop and the current feedback loop. In order to get rid of the sampling ripple voltage in dc feedback sampling voltage,

the bandwidth of voltage feedback loop has to decline. But with the drop of bandwidth the transient performance of PFC will become worse. By way of solving the contradiction many methods are put forward [1-4]. In addition the notch filter is studied [5-6]. But the notch filter can only filter the specified harmonic and has some disadvantages to feedback loop of PFC. A comb filter is also researched [7.8]. But it needs large calculating time and is not suitable for application. Anyhow, if a notch filter or comb filter is usually implemented without ripple voltage frequency adaption function. Therefore, this paper first designed the conventional PFC controller in terms of traditional small signal theory. Then a novel harmonic suppression filter with ripple voltage frequency adaption function is put forward and its feasibility is confirmed in theory. Finally the simulation results verify the theoretical analysis and the validity of the control scheme.

Design of tradition PFC feedback loop

Fig.1 shows a single-phase output inverter with three-phase input topology with three PFC circuits. Because the sum of three-phase instantaneous input power is almost dc component but the output power is ac component. According to energy conservation theory this inverter with three-phase input single-phase output topology causes large ripple voltage which usually causes high THD and the serious amplitude unbalance of three-phase current. Because three boost circuits are same and independent, then this paper only analyzes the boost circuit in phase A. In phase A PFC circuit, the input current i_a is controlled by changing the conduction time of transistor Qa. When transistor Qa is on, the power supply is short-circuited through the inductor La; when transistor Qa is turned off, the inductor current i_a cannot be interrupted abruptly and flows through diode Da, charging dc bus capacitor C.

According to the on and off state, this paper can get state-space average equation of A phase boost circuit is shown as follows:

$$\begin{cases} L_a \dfrac{di_a}{dt} = V_a - V_{dc}(1 - D_a) \\ C \dfrac{dV_{dc}}{dt} = i_a(1 - D_a) - \dfrac{V_{dc}}{Z_a} \end{cases} \qquad \text{... (1)}$$
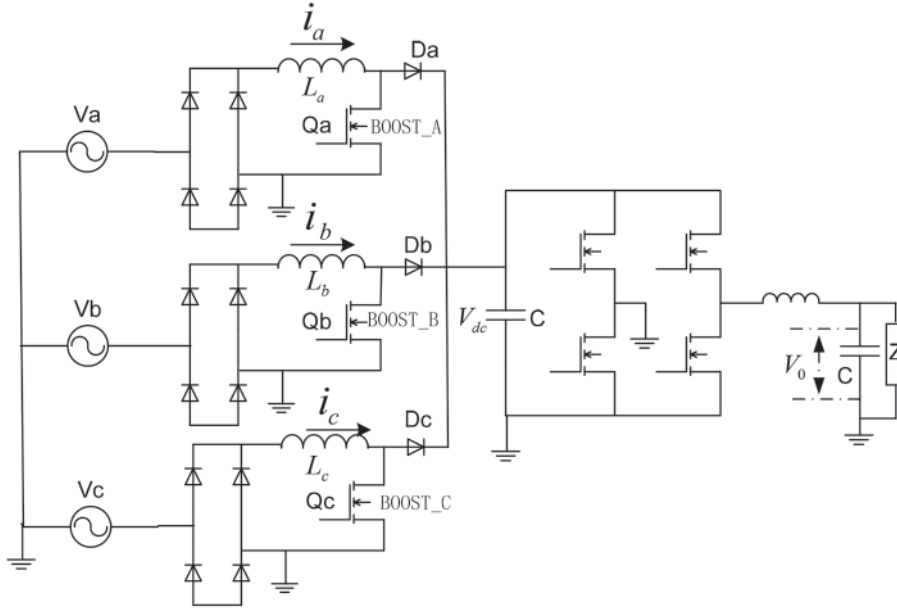
Fig.1 A single-phase output inverter with three-phase input topology with PFC function

where V_a, i_a, V_{dc}, Z_a, D_a stand for utility voltage, inductor current, dc voltage, equivalent load and duty in A phase respectively. Considering the perturbation at i_a, V_{dc} and D_a in terms of small signal theory [9,10], this paper defines $i_a = \bar{i}_a + \hat{i}_a$, $V_{dc} = \bar{V}_{dc} + \hat{V}_{dc}$, $D_a = \bar{D}_a + \hat{D}_a$, ignores the second order components and does Laplace transform to the perturbation functions. Finally the transfer of the inductor current perturbation $\hat{i}_a(s)$ to the switching perturbation $\hat{D}_a(s)$ and the transfer of dc voltage perturbation $\hat{V}_{dc}(s)$ to the inductor current perturbation can be achieved as following:

$$\begin{cases} \dfrac{\hat{i}_a(s)}{\hat{D}_a(s)} = \dfrac{(C_{dc}Z_a S + 2)\bar{V}_{dc}}{L_a C Z_a S^2 + L_a S + (1-\bar{D}_a)^2 Z_a} \\ \dfrac{\hat{V}_{dc}(s)}{\hat{i}_a(s)} = \dfrac{Z_a(1-\bar{D}_a)^2 - L_a S}{(1-\bar{D}_a)(2 + C_{dc}Z_a S)} \end{cases} \quad \text{... (2)}$$

Supposing the dc bus voltage reference is 360V, the nominal inductance L_a is 1.2mH, the dc bus capacitance C is 6000uF, the switching frequency is 20 kHz, and the total output power of three-phase PFC is 8000W. So the equation (2) can be written as following:

$$\begin{cases} \dfrac{\hat{i}_a(s)}{\hat{D}_a(s)} = \dfrac{105S + 720}{0.3499*10^{-3}S^2 + 1.2*10^{-3}S + 7.39} \\ \dfrac{\hat{V}_{dc}(s)}{\hat{i}_a(s)} = \dfrac{7.39 - 1.2*10^{-3}S}{1.22 + 0.1779S} \end{cases} \quad \text{... (3)}$$

As we all know that the PFC usually adopts double feedback loop controlling scheme to regulate the input current in phase with the input utility voltage. The output of the voltage feedback loop is V_m which represents the conductance of the total boost circuits. V_m is required to be constant value at steady state, so this paper has to damp the

dc voltage ripple by the voltage feedback loop. Usually, the band-width of the voltage feedback loop is required to be designed at about 25Hz, but too low band-width may worsen transient response. As a result, this paper makes compromise between the steady behaviour and the transient response.

The band-width of current feedback loop f_c should be smaller than the ratio between the switching frequency f_{sw} and 2π ($f_c < f_{sw}/2\pi$). Considering the delay and the nonlinear factors in the controlling system, this paper designs the band-width of the current feedback loop at around 2.5 kHz. Taking the precision of controller into account the sequence of controller is that the current loop controller should be first designed. At last for voltage loop controller an assumption should be made that the zero point ($Z_a(1-\bar{D}_a)^2/L_a$) in $\hat{V}_{dc}(s)/\hat{i}_a(s)$ is very far from virtual axis, so the influence of the zero point can be ignored in the PFC voltage feedback loop.

Because PFC is nonlinear control, we should consider input utility voltage for different phase and amplitude, different load, the inductor value in different current, and so on. Based on that, this paper should analyze its different working condition. If the controller meets the steady requirements for all the conditions mentioned above, we can say that the controller is practical. So, this paper only shows a bode plot of voltage and current loop at full resistance load condition. The voltage controller $G_v(s)$ and the current controller $G_i(s)$ are show in formula (4):

$$\begin{cases} G_v(s) = \dfrac{1270(s + 24)}{s(s + 300)} \\ G_i(s) = \dfrac{2040(s + 7200)}{s(s + 39990)} \end{cases} \quad \text{... (4)}$$

The open loop bode plot of the voltage feedback loop and the current feedback loop are shown in Figs.2 and 3 individually.

3. Digital filter for voltage feedback loop

The specified transfer function of the second-order BPF in the Laplace domain is expressed as:

$$BPF = \dfrac{k\omega_n s}{s^2 + k\omega_n s + \omega_n^2} \quad \text{... (5)}$$

Where ω_n is the natural angular frequency which should be equal to the frequency of dc voltage ripple and k is a coefficient deciding the bandwidth of the BPF.
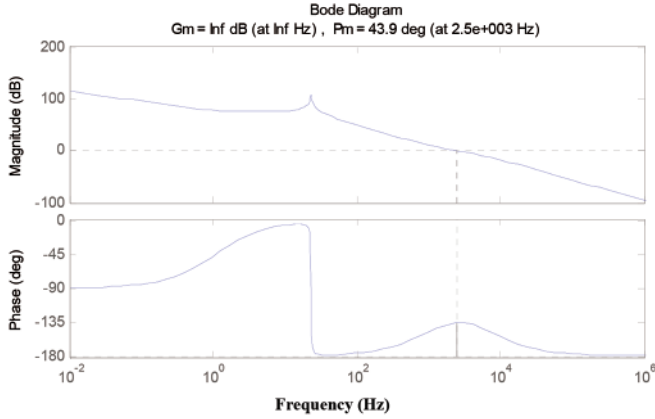
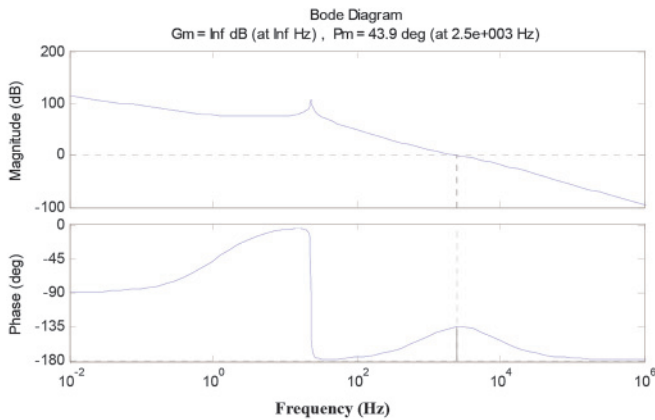Fig.2 voltage loop (open loop) bode plot

Fig.3 current loop (open loop) bode plot

Fig.4 Bode plot of the BPF with different k.

be studied so as to broaden the range of applications of the proposed dc voltage ripple filter. A full-pass filter (APF) $(s–\omega_n)/(s+\omega_n)$ is used to realize ripple frequency adaptation algorithm.

The bode plot of the APF ($\omega_n=200\pi$) is shown in Fig.6. On the assumption that an extra phase lock loop track the phase of output inverter voltage with 50Hz frequency which can cause dc voltage ripple of 200π Hz frequency in topology of Fig.1. Therefore the phase lock signal $(\cos\alpha)$ act as the input of the APF, then the output signals of the APF can be expressed as, $\cos(\alpha-\sigma)$ where σ is the delay angle of APF at ω_n is equal to 200π .

According to Fig.6, if the estimated frequency of the filter $\hat{\omega}_n$ is equal to the real frequency of dc ripple voltage, then $\cos(\alpha-\sigma)$ will be equal to $\sin\alpha$. Therefore, if the estimated frequency $\hat{\omega}_n$ is bigger than the dc voltage ripple frequency the lag phase σ will be smaller than 90º, which means that the phase of $\cos(\alpha-\sigma)$ is in front of the phase of $\sin\alpha$. On the other hand, if $\hat{\omega}_n$ is smaller than dc bus voltage ripple frequency, the lag phase σ will be larger than 90º, which means that the phase of

The bode plot of the BPF ($\omega_n=200\pi$) is shown in Fig.4. It is obvious to see that the filter shows itself as unit gain with zero phase-shift at 100Hz. the smaller value of k will have a narrower window at 100 Hz. In addition, the low frequency and high frequency utility voltage harmonics are significantly reduced rapidly with small value of k.

According to formula (5) the proposed three-phase PFC block diagram with novel filter dc eliminating voltage ripple structure is shown in Fig.5. Therefore, making use of BPF in dc bus voltage feedback loop can attenuate the dc voltage ripple synchronously.

4. DC bus voltage ripple frequency adaptation algorithm

Since the frequency of dc voltage ripple is two times the output inverter frequency in this three-phase input and single-phase output topology. If the frequency of output inverter changes the frequency of dc voltage ripple will be variable synchronously. Therefore, the parameter ω_n in BPF should be updated as soon as possible. A feasible frequency adaptation algorithm should
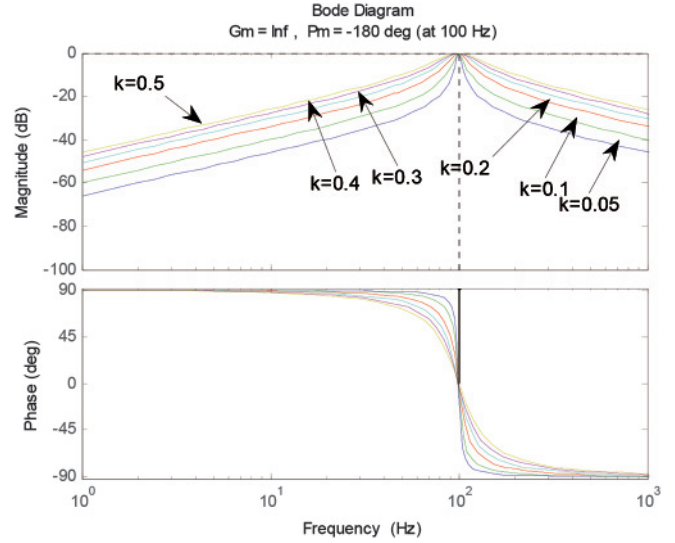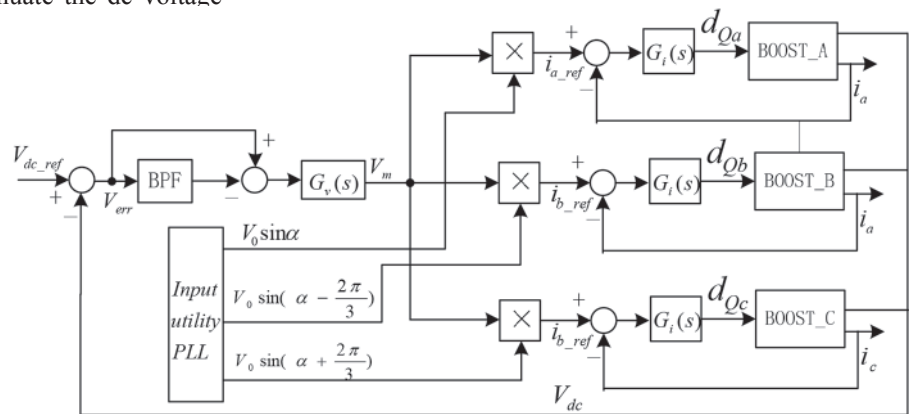

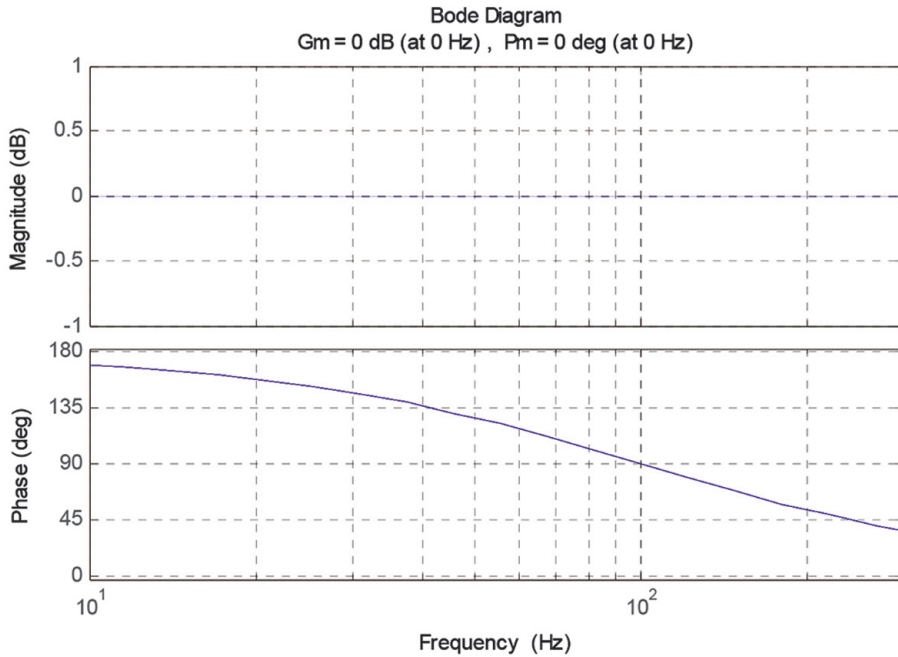Fig.5 Proposed three-phase PFC block diagram with BPF filter

Fig.6 Bode plot of APF.

cos($\alpha-\sigma$) lag behind the phase of sinα.

Then, the error between sinα and cos($\alpha-\sigma$) can be used to estimate the dc voltage ripple angular frequency at zero-crossing point of sinα adopting the following law using an integral controller, as shown in Fig.7.

Further, the dc voltage ripple frequency adaptation algorithm can be induced to the following relationship between the estimated angular frequencyand the dc voltage ripple frequency. Then, will be updated at zero-crossing point of.

$$\hat{\omega}_n = \omega_f + \frac{k_i sign[\sin\alpha - \cos(\alpha-\sigma)]}{s}[\sin\alpha - \cos(\alpha-\sigma)]...(6)$$

Where the dc voltage ripple frequency ω_f is only a feed-forward component, and k_i is the integral coefficient for the frequency adaption feedback loop. At positive zero crossing point the integral coefficient for the frequency adaption feedback loop is k_i, otherwise at negative zero crossing point the integral coefficient for the frequency adaption feedback loop is $-k_i$. The frequency adaptation integral controller calculates twice at every utility period.

Therefore, the control block diagram of the new dc voltage ripple filter arithmetic with frequency adaptation function for the three-phase PFC topology in Fig.1 is shown in Fig.8.

With the help of the new dc voltage filter the ac component is cancelled in from the dc sampling voltage and the pure dc component is reserved. Therefore, for the voltage feedback loop of PFC the effect
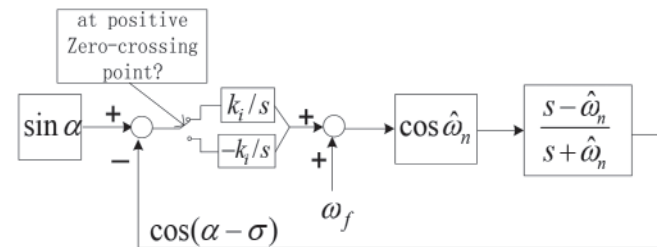

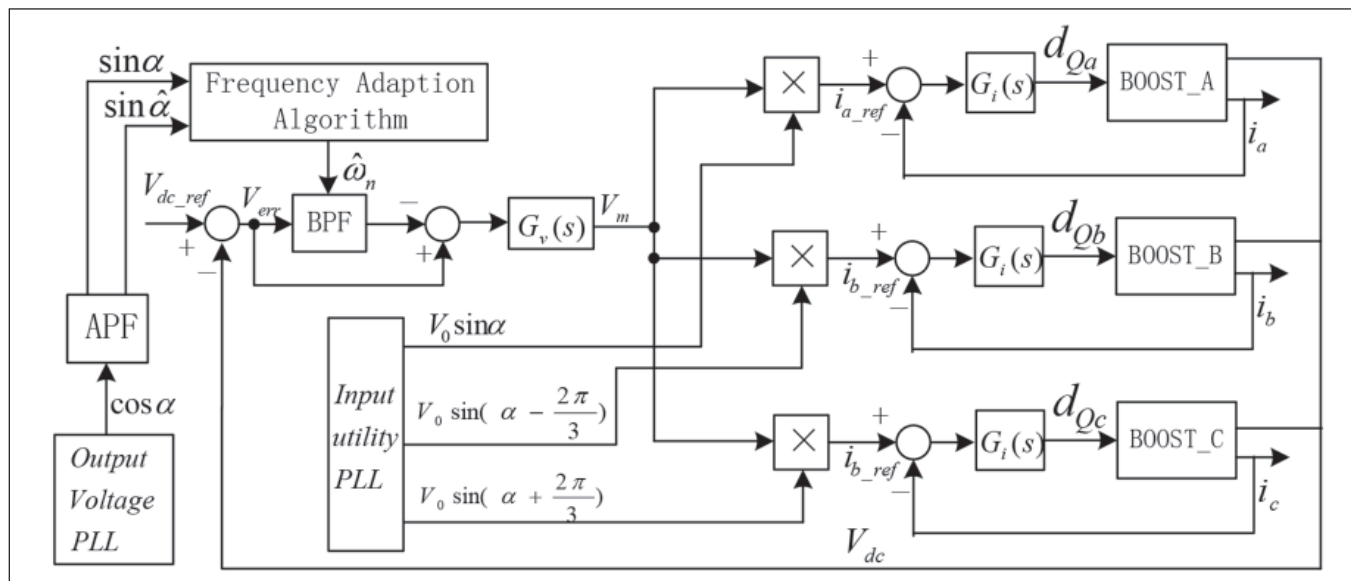Fig.7 DC voltage ripple frequency adaptation algorithm

Fig.8 Control block diagram of the new dc voltage ripple filter with frequency adaption arithmetic
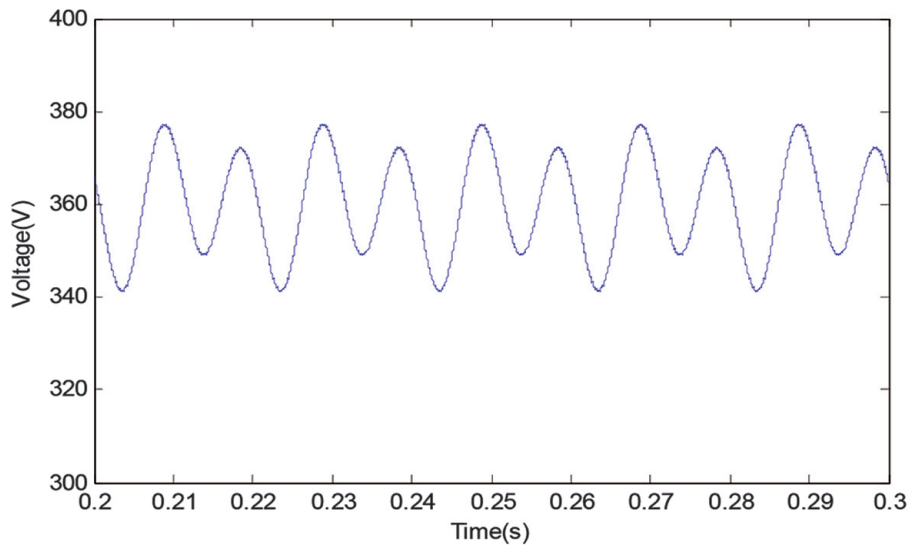
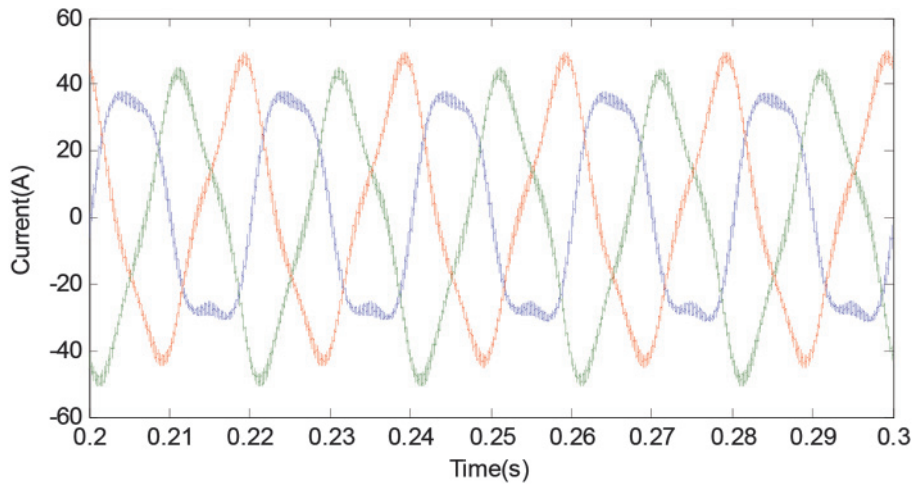Fig.9 DC voltage waveform at 100Hz dc voltage ripple

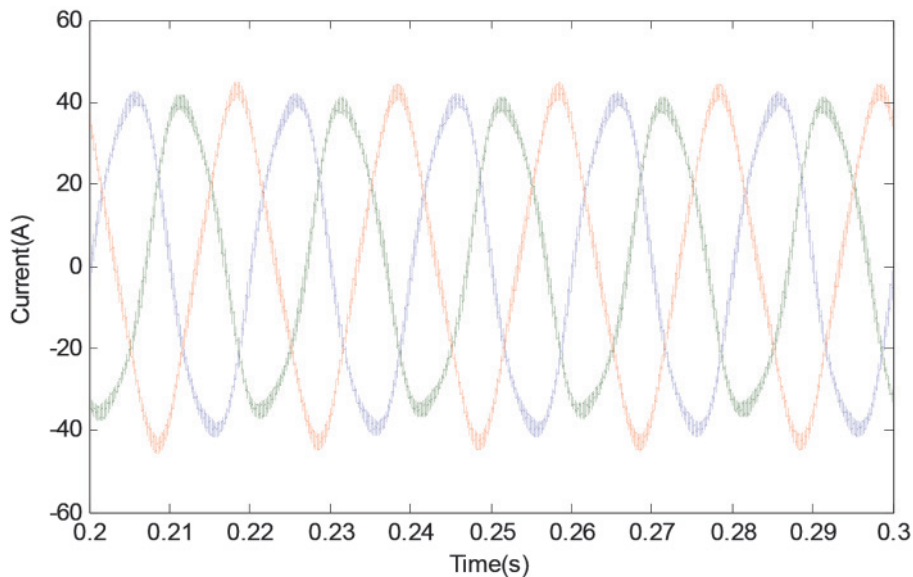Fig.10 50Hz three phase input current waveform without the filter

Fig.11 50Hz three phase input current waveform with the filter

influenced by the dc voltage fluctuating is eliminated.

5. Simulation

In order to verify the proposed algorithm, simulations are implemented by the S-function in Matlab/Simulink. The main simulation parameters are same as mentioned above, in addition, the coefficient k in BPF is 0.1, the integral coefficientin frequency adaption is 0.6. To show the promising behaviours of the proposed method, two different utility frequency operation conditions are considered in the following simulation.

As has been mentioned above, an inverter with three-phase input and single-phase output has been built by Matlab/Simulink combined with controller written by C language to verify the analysis. Fig.9 shows the dc voltage waveform on the condition of 50Hz utility. Figs.10 and 11 show the difference of three phase 50Hz input current removing or adding the dc voltage filter. Fig.12 shows the dc voltage waveform on the condition of 55Hz utility. Figs.13 and 14 show the difference of three phase 55Hz input current removing or adding the dc voltage filter.

According the simulation waveforms the proposed dc voltage ripple filter has satisfactory performances at different frequency of dc ripple voltage.

6. Conclusion

This paper puts forward a novel three-phase dc voltage ripple filter with ripple voltage frequency adaption function in order to suppress the large dc voltage ripple for dc voltage feedback loop of PFC. The proposed filter can eliminate the ac component in sampling dc voltage and simplify the design of the PFC voltage feedback loop. The filter only need small calculation and can be carried out easily. Finally the simulation results verify the control scheme.
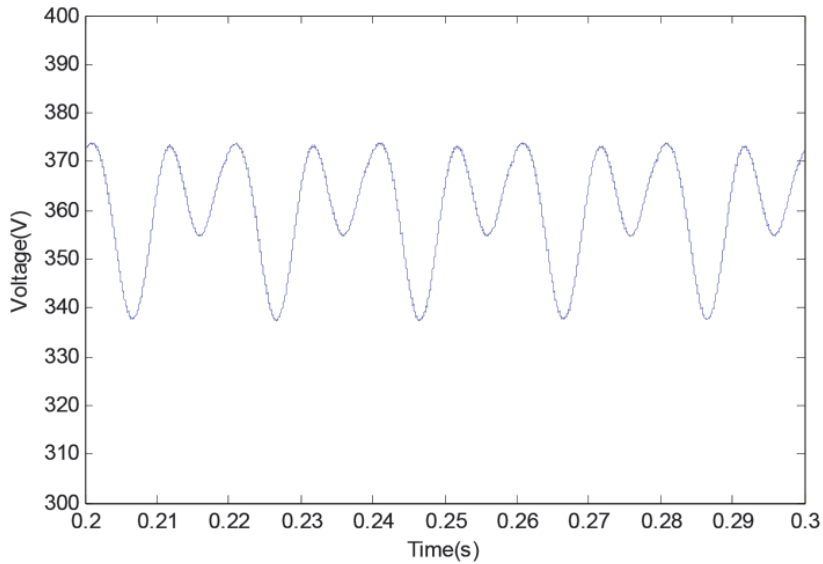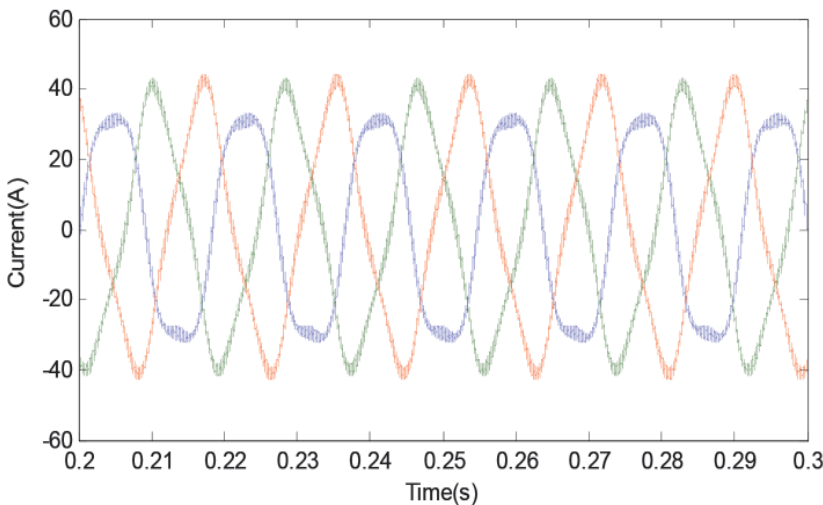
Fig.12 DC voltage waveform at110Hz dc voltage ripple

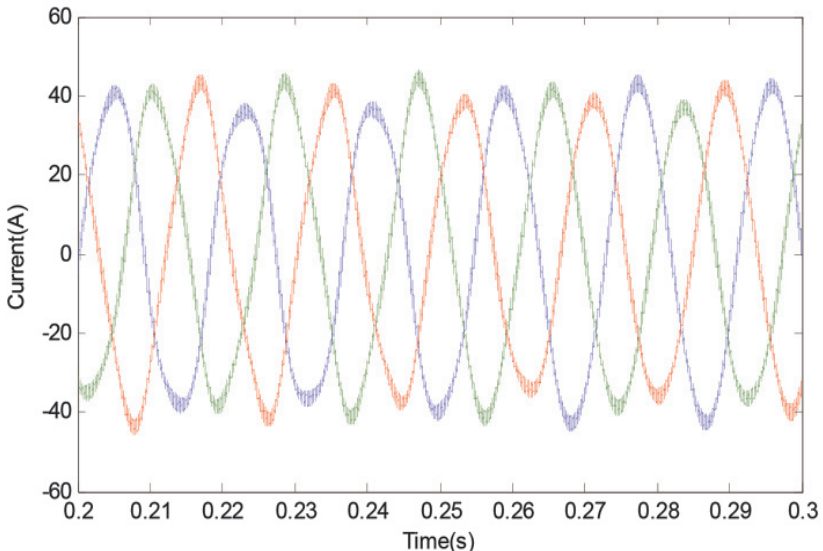Fig.13 55Hz three phase input current waveform without the filter

Fig.14 55Hz three phase input current waveform with the filter

7. References

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