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A new half-cascaded multilevel inverter topology to improve systems performance parameters

This paper presents the performance analysis of a half-cascaded multilevel inverter topology. The inverter consist of a new nine-level hybrid inverter with less number of switches. A carrier based level shifted PWM (LS-PWM) technique have been used to generate the output waveforms of the proposed multilevel inverter. The modulation index of the multilevel inverter has been controlled to control the output voltage of the inverter. The validation of the model is done in MATLAB/SIMULINK environment. The simulation results of the inverter output voltage, load current and the % total harmonic distortion (THD) of the proposed nine-level inverter at different modulation index is presented. The comparison of the proposed multilevel configuration with conventional cascaded H-bridge multilevel inverters for same number of voltage levels.

Keywords: *MLI; LS-PWM; THD.*

I. Introduction

Multilevel inverters (MLI) are becoming popular in medium and high power applications [10], [13] due to its numerous advantages like the multilevel inverter provides better output waveform quality with lower dv/dt, reduced harmonics and loss etc. In recent years, the multilevel inverters have emerged as the most popular interface for the photovoltaic system energy sources [4-5], [7], [14]. Multilevel inverters are used for numerous applications like micro grid system [1-2], power system [5] distributed generation [3-4], adjustable speed drives and static and reactive power compensation [6-7]. In recent years, different multilevel inverter configurations have been developed and also several sub topologies and hybrid topologies have been introduced [8]. There are three classic types of multilevel inverter topology: like a diode clamped or neutral point clamped (NPC) multilevel inverter [9], capacitor clamped or flying capacitor multilevel inverter (FCMLI) [10] and cascaded H-Bridge multilevel inverter (CHB-MLI) [11]. The performance of multilevel inverters is also depends on the modulation strategy used. In [12-13] a number of carrier based pulse width modulation (PWM) techniques have been presented for the various multilevel inverters to increase the efficiency and improve the inverter output waveform.

A new topology of generalized multilevel inverter is proposed in this paper, which is commonly suited for the high number of voltage levels (five or more than five levels) associated with a less number of power switches. This also reduces the number of gate driver circuits and relevant hardwires. By considering the same number and value of DC sources, the proposed inverter topology can generate more number of voltage level compared to the classic multilevel inverter topologies as discussed in the next section. The exhaustive simulation results of the proposed nine-level will be presented later.

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II. Proposed multilevel inverter topology

In all popular classic multilevel inverter configurations, the required number of components depend on the number of output voltage levels. The switches and related gate drive circuits are the main components in the structure of multilevel converters. With an increase in the components, the inverter circuit size and the cost increase, also, the control scheme gets complicated.

The proposed topology is a generalized inverter structure cascading several two-level inverter module that consist of two switches and one DC source as shown in Fig.1. Several two-level modules can be incorporated or cascaded in the

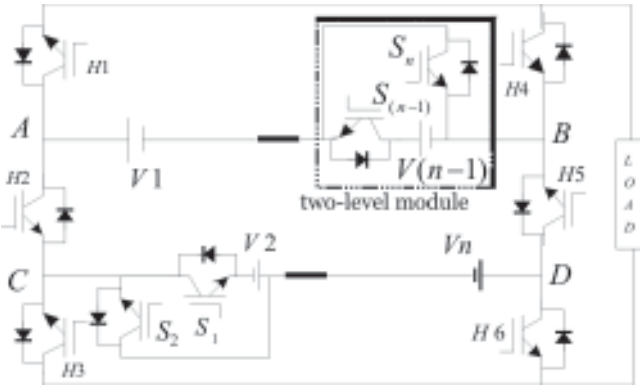

Fig.1 Generalized circuit diagram of the proposed n–level half cascaded inverter

upper arm (AB) or the lower arm (CD) as shown in Fig.1, to increase the voltage levels. Each module can increase the number of voltage levels of the inverter by two (one positive and one negative voltage levels).

A nine-level inverter with this configuration, as shown in Fig.2, have ten switches which are capable of generating output voltage of nine levels; hence, the number of switches is reduced. Out of the ten switches, three switches are used in each leg (AC and BD) of the inverter and the rest of the switches are used to the arm of converter for increasing the voltage levels. The four DC voltage sources labelled as V1, V2, V3 and V4 are taken with equal magnitude of 100V each, in this work. The switches of the inverter legs are labelled as H1, H2, H3, H4, H5, H6 while the switches in the arms of the inverter (AB and CD) are labelled as S_1, S_2, S_3 and S_4.

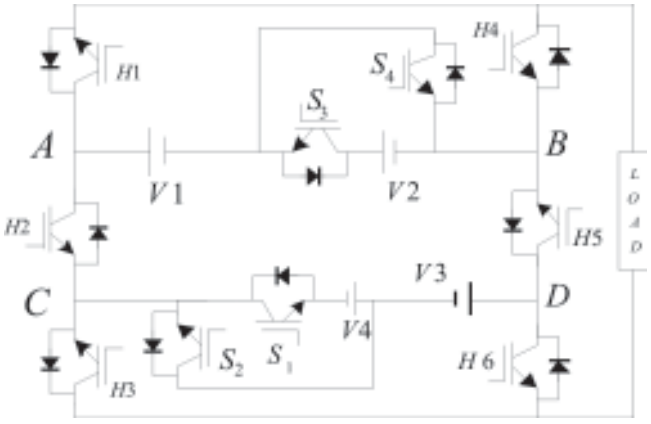

Fig.2 Circuit diagram of the proposed nine –level half cascaded inverter

Table I shows the output voltage levels of the above nine-level inverter with the switching status of the switches. It is clearly observed from the table that to obtain any particular dc voltage level, only five switches have to be turned on simultaneously compared to the six switches in a cascaded H-bridge multilevel inverter with equal voltages.

This topology works well even when the load is highly inductive or resistive. There is an equal distribution of dc voltage, stress in every switches, power losses is reduces also the power rating of IGBT is decreases. Since the number of switching devices is less than the classic multilevel inverter (NPC, CHB-MLI and FCMLI), the overall losses will be lesser than the classic MLI at same operating conditions. The comparison of the proposed inverter performance with the CHB-MLI is given in section-4.

III. Level shifted PWM for the proposed nine-level inverter

The numerous modulation techniques are reported for the control of multilevel inverter like carrier based level shifted pulse width modulation technique (LS-PWM) [11-12], phase shifted PWM (PS-PWM) [8], [14], space vector PWM (SVPWM) [15-16] etc. A carrier level shifted PWM technique [12] has been adopted in this paper for generating switching states of the multilevel inverter. For a nine-level inverter, eight triangular carrier signals with their magnitude is off-set in such a way that, they are shifted vertically. These carrier signals are compared to the reference sinusoidal signal (V_{ref}) to generate the respective switching states as shown in Fig.3. The carrier signals have the same frequency, same peak amplitude (V_{cr}) and are in same phase, but, there is a level shift between them. In the positive half cycle, if the amplitude of reference signal is greater than that of carrier wave, then the output is defined as positive high, else zero. Similarly, in negative half cycle, if the reference signal is smaller than that of carrier, the output is negative high, else zero. The magnitude of the inverter voltage can be adjusted by controlling the reference voltage (V_{ref}) or the modulation index of the PWM. The modulation index (M_i) of the LS-PWM for the nine-level inverter can be represented as:

$$M_i = \frac{V_{eref}}{4V_{cr}} \quad \text{... ... (1)}$$

IV. Comparison between proposed and cascaded H-bridge MLI

A comparative analysis between the proposed inverter and the conventional cascaded H-bridge MLI is done and presented here in Table II. The proposed inverter circuit needs a lower number of power devices than the traditional

TABLE I VALID SWITCHING STATES FOR PROPOSED MLI TOPOLOGY

Output voltage (V_o) and the corresponding switching status of the proposed nine-level inverter with (V1=V2 =V3=V4=V_{dc})										
Vo	S1	S2	S3	S4	H1	H2	H3	H4	H5	H6
$4V_{dc}$	1	0	1	0	0	1	0	1	0	1
$3V_{dc}$	0	1	1	0	0	1	0	1	0	1
$2V_{dc}$	0	1	0	1	0	1	0	1	0	1
V_{dc}	0	1	0	1	0	1	1	1	0	0
0	0	0	0	0	0	0	0	1	1	1
$-V_{dc}$	0	1	0	0	0	0	1	1	1	0
$-2V_{dc}$	0	1	0	1	1	0	1	0	1	0
$-3V_{dc}$	0	1	1	0	1	0	1	0	1	0
$-4V_{dc}$	1	0	1	0	1	0	1	0	1	0

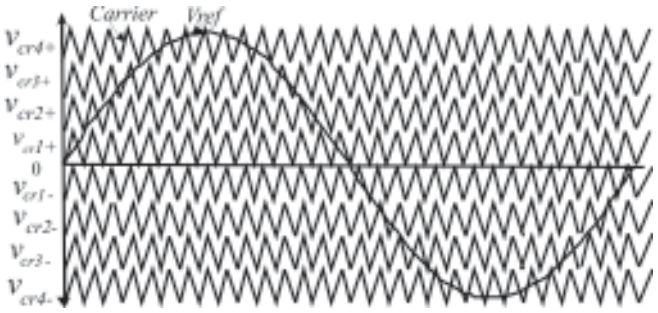

Fig.3 Comparison of carriers and reference signal in LS-PWM of the proposed nine-level inverter

TABLE II COMPARISON BETWEEN TRADITIONAL CASCADED MLI AND THE PROPOSED INVERTER

Traditional cascaded MLI	Proposed MLI
Nine levels are achieved using 16 switches.	Nine levels are achieved using ten switches only.
Requires more switches and control hardware.	Such topology requires less switches and less hardware and hence cheaper.
Higher switching losses	Overall switching losses are less

cascaded inverter. This will sufficiently reduce the cost of the high level inverter and reduce the switching components, filter requirements and improve the efficiency of the energy conversion.

V. Simulation Results

An exhaustive simulation of the proposed nine-level inverter have been done in MATLAB/Simulink platform to test the performance of the inverter at different modulation index (M_i). The switching frequency of the inverter is considered as 5.0 kHz (F_s=5.0 kHz) and the magnitude of the DC voltage sources (V_{dc}) are equal to 100V for the R-L load. Figs.4-5 show the simulation results of the output voltage, stator current at different modulation index.

From the Fig.4(a), it is clearly observed the nine voltage levels are obtained ranging from +400 V to -400 V. The % total harmonic distortions (THD) of the output voltage is also considered and presented in Fig.4(a).

From the Fig.4(a) it is also observed that, the dominant harmonic components are generated around the switching frequency of the inverter and its multiple (F_s, $2F_s$, …). The low order harmonic components are very low and are negligible. Therefore, the output currents can be easily filtered out by the inductance of the load itself and is sinusoidal as shown in Fig.4(b).

Fig.5 represents the output voltage and current waveforms of the nine level half-cascaded inverter with R-L load at a lower modulation index equal to 0.6. At lower modulation index the inverter output voltage levels are decreased proportionally to the reference voltage of the level-shifted PWM (LS-PWM) controller.

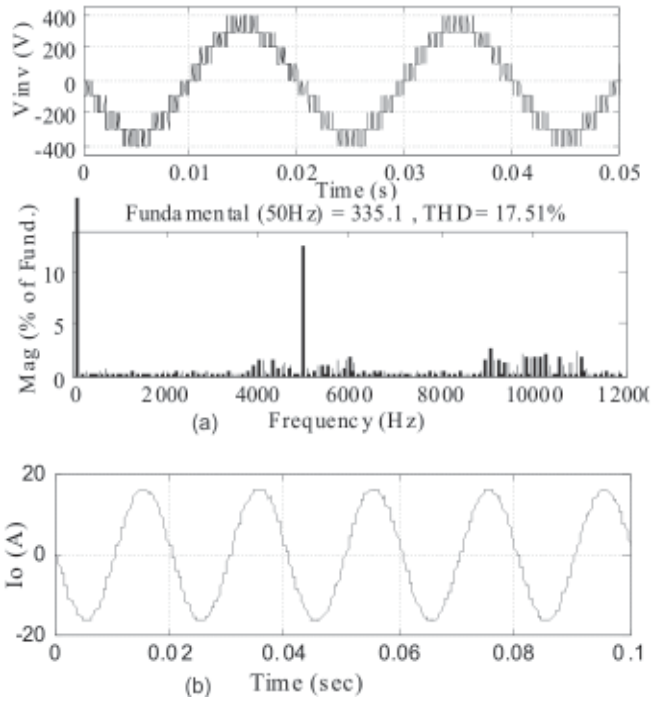

Fig.4 Simulation results of the nine-level half cascaded inverter at M_i=0.9 (a) output voltage of the inverter (Vinv) and its % THD and (b) the load current

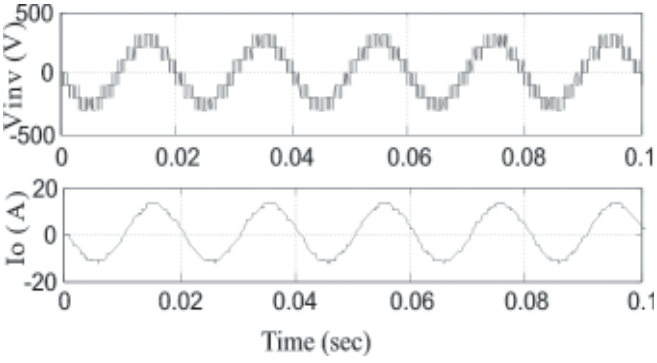

Fig.5 Output voltage and the load current of the nine-level Half cascaded inverter at modulation index M_i = 0.6

VI. Conclusions

In this paper, a new generalized half-cascaded multilevel inverter structure is proposed and simulated for the nine-level inverter. In the proposed structure, less number of power electronic switches are used that not only reduced the size, weight and cost of the circuit but also reduces the switching losses. The functionality of the proposed inverter structure has been verified in the MATLAB/Simulink platform. The simulation results of the inverter output voltage and currents at different modulation index are presented. The harmonic analysis is also incorporated in the paper. The simulation results clearly show that the proposed topology can effectively work as a multilevel inverter with a reduced number of switches compared to the conventional inverter.

References

[1] Yu, X., Wang, H., Khambadkone, A. M. (2010): 'Control of paralleled PEBBsto facilitate the efficient operation of microgrid'. Proc. IEEE ISIE, Bari, Italy, July, pp. 2217–2222.

[2] Ye, Z., Jain, P. K., Sen, P. C. (2007): 'Circulating current minimization in high-frequency ac power distribution architecture with multiple inverter modules operated in parallel', *IEEE Trans. Ind. Electron*., 54, (5), pp. 2673–2687.

[3] Guerrero, J. M., Matas, J., de Vicuña, L. G., Castilla, M., Miret, J.(2006): 'Wireless-control strategy for parallel operation of distributed generation inverters', *IEEE Trans. Ind. Electron.*, 53, (5), pp. 1461–1470.

[4] Romero-Cadaval, E., Milanes-Montero, M. I., Gonzalez-Romera, E., Barrero-Gonzalez, F. (2009): 'Power injection system for grid-connected photovoltaic generation systems based on two collaborative voltage source inverters', *IEEE Trans. Ind. Electron*., 56, (11), pp. 4389–4398.

[5] Turner, R., Walton, S., Duke, R.(2010): 'Stability and bandwidth implications of digitally controlled grid-connected parallel inverters', *IEEE Trans. Ind. Electron*., 57, (11), pp. 3685–3694.

[6] Kadir, M.N.A., Mekhilef, S., Ping, H.W. (2010): 'Voltage vector control of a hybrid three-stage eighteen-level inverter by vector decomposition', *IET Trans. Power Electron*., 3, (4), pp. 601–611.

[7] Daher, S., Schmid, J., Antunes, F. L. M. (2008): 'Multilevel inverter topologies for stand-alone PV systems', *IEEE Trans. Ind. Electron.*, 55, (7), pp. 2703–2712.

[8] Sadigh, A.K., Hosseini, S.H., Sabahi, M., Gharehpetian, G.B. (2010): 'Double flying capacitor multicell converter based on modified phase-shifted pulse width modulation', *IEEE Trans. Power Electron.*, 25, (6), pp. 1517–1526.

[9] Rodriguez, J., Bernet, S., Steimer, P., Lizama, I. (2010): 'A survey on neutral point-clamped inverters', *IEEE Trans. Ind. Electron.*, 57, (7), pp. 2219–2230.

[10] Dargahi, V., Sadigh, A.K., Abarzadeh, M., Pahlavani, M.R.A., Shoulaie, A. (2012): 'Flying capacitors reduction in an improved double flying capacitor multicell converter controlled by a modified modulation method', *IEEE Trans. Power Electron.*, 27, (9), pp. 3875–3887.

[11] Mohamad Reza Banaei, Mohammad Reza Jannati Oskuee, Hossein Khounjahan (2014): "Reconfiguration of semi-cascaded multilevel inverter to improve systems performance parameters" *IET Power Electron.*, 7, (5), pp. 1106–1112.

[12] Tolbert, L. M., Habetler, T. G. (1999): 'Novel multilevel inverter carrier based PWM methods', *IEEE Trans. Ind. Appl.*, 35, (5), pp. 1098–1107.

[13] Franquelo, L. G., Rodriguez, J., Leon, J. I., Kouro, S., Portillo, R., Prats, M.M. (2008): 'The age of multilevel converters arrives', IEEE Ind. Electron. Mag., 2, (2), pp. 28–39.

[14] Patrao, I., Garcerá, G., Figueres, E., González-Medina, R. (2014): 'Grid-tie inverter topology with maximum power extraction from two photovoltaic arrays', *IET Renew. Power Gener.*, 8, (6), pp. 638-648.

[15] Jana, K.C., Biswas, S.K, and Kar Chowdhury, S. (2013): 'Performance evaluation of a simple and general space vector pulse-width modulation-based M-level inverter including over-modulation operation', *IET Power Electron.*, 6, (4), pp. 809–817.

[16] Jana, K.C., Biswas, S.K. (2015): "A Generalized Switching Scheme for a SVPWM based N-level Inverter with Reduced Switching Frequency and Harmonics", IET Power Electron., 8, (12), pp. 2377–2385.